REMARKS

I.   Introduction

In response to the pending Office Action, Applicants have incorporated a limitation of claim 2 into claim 1. In addition, new claim 9 has been added. Claim 2 has been cancelled, without prejudice. Claims 3, 4 and 6-8 have been amended to overcome § 112 rejections and to correct claim dependency. Figs. 23-26 have been amended to include the legend "Prior Art". No new matter has been added.

Applicants respectfully submit that all pending claims as currently amended are patentable over the cited prior art.

II.   The Rejection Of Claims 1-4, 7 And 8 Under 35 U.S.C. § 112

Claims 1-4, 7 and 8 stand rejected under 35 U.S.C. § 112, second paragraph, for being indefinite. The claimed limitations of "silicon", "the silicon" and "germanium" were unclear as to which of these elements they referred.

In response, Applicants have amended claim 1 to recite "where a composition ratio of the germanium to the silicon in the composition-ratio graded base layer varies in a thickness direction of the composition-ratio graded base layer" and claims 3 and 7 to include the term "silicon-germanium" to clarify the claims. As such, Applicants respectfully request that the § 112 rejection be withdrawn.

III.   The Rejection Of Claims 1-4, 7 and 8 Under 35 U.S.C. § 103

Claims 1-4, 7 and 8 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the Applicant's Admitted Prior Art ("AAPA"). Applicants respectfully traverse this rejection of the pending claims for at least the following reasons.

Amended independent claim 1 recites a bipolar transistor comprising a substrate, a intrinsic base region having a silicon buffer layer comprised of silicon which is formed on said substrate, and a composition-ratio graded base layer which is formed on the silicon buffer layer and comprises silicon and at least germanium. The composition ratio of the germanium to the silicon in the composition-ratio graded base layer varies in a thickness direction of the composition-ratio graded base layer. An extrinsic base region having an extrinsic base formation layer is comprised of silicon which is formed on the substrate and adjacent to the silicon buffer layer. In addition, a thickness of the extrinsic base formation layer is substantially equal to a thickness of the silicon buffer layer, each of the extrinsic base formation layer and the silicon buffer layer has a thickness of not less than 40nm, and a surface of the extrinsic base formation layer is silicided.

It is alleged that the AAPA, in Fig. 24, teaches that a surface of the extrinsic base formation layer is silicided. However, as can be seen in Fig. 24, the extrinsic base formation layer 113, which is formed concurrently with the silicon buffer layer 109 of the intrinsic base region 106, is covered with the second 114, third 115 and fourth 116 layers. Only the fourth layer 116 is silicided with a silicon layer 108. In contrast, as shown in Fig. 2 of the drawings, the extrinsic base formation layer 113 is silicided with a Co silicide layer 19. As such, the AAPA does not disclose that a surface of the extrinsic base formation layer is silicided.

Moreover, it is also admitted that the AAPA does not disclose that each of the extrinsic base formation layer and the silicon buffer layer has a thickness of not less than 40 nm. However, it is alleged that it would be obvious for one skilled in the art to have each of the extrinsic base formation layer and the silicon buffer layer have a thickness of not less than 40 nm. Applicants respectfully disagree.

It is well known in the art that commonly, a thickness of a silicon buffer layer 109 is set to about 10 nm to 20 nm. For example, as discussed in paragraph [0090] the present specification:

> "The Si buffer layer 109 of the bottom layer in the intrinsic base region 11 does not function as device but is purposed to stabilize crystal growth of the non-dope SiGe spacer layer 110, as an upper layer of the Si buffer layer 109. So, thickness of the Si buffer layer 109 of approximately 10nm to 20nm is generally considered enough to fulfill its function."

As a further example of support that the thickness of the Si buffer layer is typically about 10-20 nm, Attachment 1 – "On the Potential of SiGe HBTs for Extreme Environment Electronics" (p. 1562) is included with this Amendment. As is shown in the document, one role of the Si buffer layer is to cover contamination on a Si substrate surface to epitaxially grow a high quality SiGe crystal stably. While a thick layer is favorable, all that is needed to accomplish this is several nm of thickness.

However, another role of the Si buffer is to insert a non-doped high-resistance layer between a SiGe base and a Si collector (inside substrate) to reduce a base-collector electric field and increase voltage resistance of a transistor. Since the voltage resistance of the transistor increases as the thickness of the Si buffer layer increases, the travel distance of the electrons increases as well, resulting in a slow operation speed. Commonly, the trade off between the two conflicting roles lies in a Si buffer thickness of 10-20 nm.

In contrast, the present disclosure features that the thickness of the extrinsic base formation layer is specifically verified, thereby leading to a thickness much different than that of

conventional silicon layers, as discussed in paragraphs [0090]-[0098] of the specification. Thus, the above-mentioned conventional thickness does not apply. As such, it is only in view of improper hindsight reasoning from a review of the specification that the Examiner would find that a skilled artisan would choose thicknesses as recited in claim 1 of the present disclosure. Accordingly, the AAPA fails to disclose all of the limitations of claim 1.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. As is clearly shown, the AAPA does not disclose a bipolar transistor comprising an extrinsic base region having an extrinsic base formation layer comprised of silicon which is formed on said substrate and adjacent to the silicon buffer layer, wherein a thickness of the extrinsic base formation layer is substantially equal to a thickness of the silicon buffer layer, and each of the extrinsic base formation layer and the silicon buffer layer has a thickness of not less than 40nm. Accordingly, Applicants submit that the AAPA does not render claim 1 of the present disclosure obvious and as such, claim 1 is patentable and allowable over the cited prior art. Accordingly, Applicants respectfully request that the § 103(a) rejections of claim 1 be withdrawn.

IV. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

V.   Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that

all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is

hereby made. Please charge any shortage in fees due in connection with the filing of this paper,

including extension of time fees, to Deposit Account 500417 and please credit any excess fees to

such deposit account.

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On the Potential of SiGe HBTs for Extreme Environment Electronics

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Invited Paper

"*Extreme environments*" *represents an important niche market for electronics and spans the operation of electronic components in surroundings lying outside the domain of conventional commercial, or even military, specifications. Such extreme environments would include, for instance, operation to very low temperatures (e.g., to 77 K or even 4.2 K), operation at very high temperatures (e.g., to 200 °C or even 300 °C), and operation in a radiation-rich environment (e.g., space). We argue that the unique bandgap-engineered features of silicon–germanium heterojunction bipolar transistors offer great potential to simultaneously satisfy all three extreme environment applications, potentially with little or no process modification, ultimately providing compelling cost advantages at the IC and system level.*

Keywords—Cryogenic temperatures, extreme environments, high temperatures, radiation, silicon–germanium heterojunction bipolar transistor (SiGe HBT), silicon–germanium (SiGe).

I. INTRODUCTION

During the past several years, silicon–germanium heterojunction bipolar transistor (SiGe HBT) technology has entered the global semiconductor electronics market with a bang, and SiGe HBT technologies are being increasingly deployed by a host of companies in the North America, Europe, and the Far East for a wide variety of communications circuit applications [1]. Progress in SiGe HBT device performance has proceeded at a truly dizzying pace. Unlike for CMOS technology "nodes," which are based solely on lithographic gate length dimensions, SiGe HBTs, being vertical transport devices whose overall performance
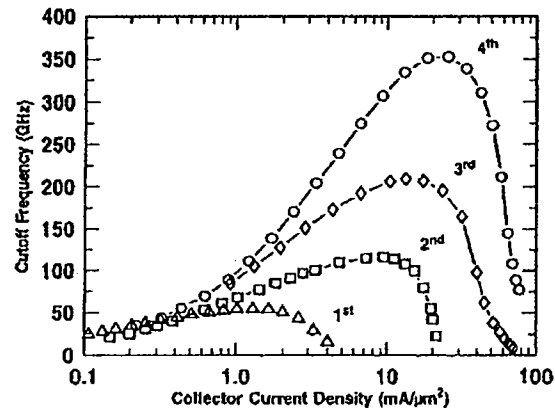
Table 1
Representative SiGe HBT Parameters for Three Distinct SiGe HBT BiCMOS Technology Generations

Parameter	First	Second	Third
$W_{B,eff}$ (nm)	0.42	0.18	0.12
peak β	100	200	400
V_A (V)	65	120	> 150
BV_{CEO} (V)	3.3	2.5	1.7
BV_{CBO} (V)	10.5	7.5	5.5
peak f_T (GHz)	47	120	207
peak f_{max} (GHz)	65	100	285

Fig. 1. Unity-gain cutoff frequency as a function of bias current for four generations of commercially available SiGe HBT technology.

is more closely tied to the vertical profile (and the resultant Ge profiles used), are more conveniently defined by their transistor-level maximum small-signal frequency response. Hence, a first-generation SiGe HBT has a peak unity-gain cutoff frequency (f_T) of about 50 GHz, a second-generation SiGe HBT has a peak f_T of 100–120 GHz, and a third-generation SiGe HBT has a peak f_T in the 200-GHz range, as detailed in Table 1 and Figs. 1 and 2 [2]. The record peak f_T at the research level is at present above 350 GHz [3],
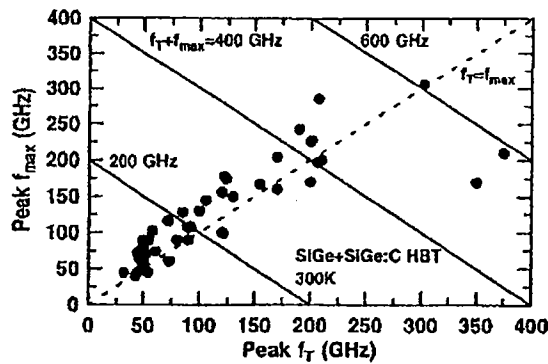
Fig. 2. Measured maximum oscillation frequency versus cutoff frequency for a variety of SiGe HBT technology generations.

and there is no immediate end in sight to this dramatic rise in device-level performance. Commercial SiGe HBTs offer transistor-level performance metrics which are quite competitive with the best III–V technologies (GaAs or InP), while maintaining strict fabrication compatibility with low-cost, high-yield Si CMOS foundry processes on large (200-mm and soon 300-mm) wafers. Thus, SiGe HBT technology effectively marries III–V-like device performance with the compelling economy of scale of Si IC manufacturing.

Robust (meaning manufacturable, at high yield) first-generation SiGe HBT technologies exist in upwards of two dozen companies worldwide (e.g., [4]), second-generation SiGe technologies in eight to ten companies (e.g., [5]), and third-generation SiGe technologies in four to five companies (e.g., [6]). The first prototype fourth-generation (300 GHz f_T + 300 GHz f_{max}) SiGe technology has been reported in 2004 [7]. The numbers of SiGe "players" is climbing rapidly worldwide. As almost universally practiced today, SiGe technology exists in a BiCMOS implementation (SiGe HBT + Si CMOS), and as an "adder" module to a core CMOS technology, which conveniently facilitates using the SiGe HBT where it offers the most advantage (i.e., in analog, RF, microwave, and very high speed digital circuits), and using the Si CMOS to its strongest advantage in highly integrated, lower performance memory and circuits (e.g., as might be found in baseband processing for wireless transceiver applications) [8]. At present, the commercial applications of SiGe HBT BiCMOS technology rest squarely in the domain of "mixed-signal" ICs, which in general incorporate analog and RF/microwave/millimeter-wave circuit functions, and the required passive elements and interconnects to implement them, together with highly integrated digital circuit functionality, presumably within the same IC technology (in this case, SiGe HBT BiCMOS), and perhaps even on the same die, to cost-effectively realize either system-on-a-chip (SoC) or system-in-a-package (SiP) solutions. The commercial market for such mixed-signal ICs is exploding, in the ever-expanding quest to build the requisite electronic infrastructure for the emerging 21st century communications revolution.

II. EXTREME ENVIRONMENT ELECTRONICS

Given this highly encouraging picture of the maturation and deployment of SiGe ICs in a variety of commercial communications applications, and its emerging pervasiveness in the electronics industry as a whole, it becomes very logical to wonder if SiGe technology can be simultaneously extended to support an even wider class of electronics applications, so-called niche applications for which market volume may in fact be small, but whose end users are nevertheless very important, and the value-add of the electronic components can be substantial. Such niche applications can often place much more demanding constraints on the electronic component building blocks than faced by commercial IC manufacturers, and hence often require significant modification of the standard foundry IC processes, at a very large and highly undesirable cost.

"Extreme environments" represent such a class of niche electronics applications. The broad class of extreme environments can be loosely defined as operation of electronic components in surroundings outside the domain of conventional commercial, or even military, specifications. Such extreme environments would include, for instance, temperatures either above or below the standard mil-spec $-55°C$ to $125°C$ temperature range (0 °C to 85 °C for commercial applications), in a radiation intense environment such as space, in a high-vibration (shock) environment, in a high- (or low-) pressure environment, and even in a caustic or chemically corrosive environment (e.g., inside the human body). For the purposes of this paper, we confine ourselves to the three most important extreme environment electronics scenarios: 1) operation to very low temperatures (e.g., to 77 K); 2) operation at very high temperatures (e.g., to 300 °C); and 3) operation in a radiation-rich environment (e.g., space).

At present, cryogenic electronics represents a small but important niche industry, with applications such as high-sensitivity cooled sensors and detectors, semiconductor–superconductor hybrid systems, space electronics, and eventually cryogenically cooled computer systems. The high-temperature operation of electronic devices and systems represents an important emerging niche industry, and embodies applications in automobiles, heavy vehicles, power switching, engine electronics, aerospace (e.g., the "all electric aircraft"), shipping, oil well logging, nuclear power, planetary space missions, and radar systems [S6]. There are currently two recent but rapidly growing thrusts within the space electronics community: 1) the use of commercial-off-the-shelf (COTS) parts whenever possible for space-borne systems as a cost-saving measure and 2) the use of SoC integration to lower chip counts and system costs, as well as simplify packaging and lower total system launch weight. The "holy grail" in the realm of space electronics can thus be viewed as a conventional terrestrial IC technology with a SoC capability, which is also radiation-hard as fabricated, without requiring any additional process modifications or layout changes. As will be argued in this paper, SiGe HBT technology embodies great potential to simultaneously satisfy all three extreme environment applications, potentially
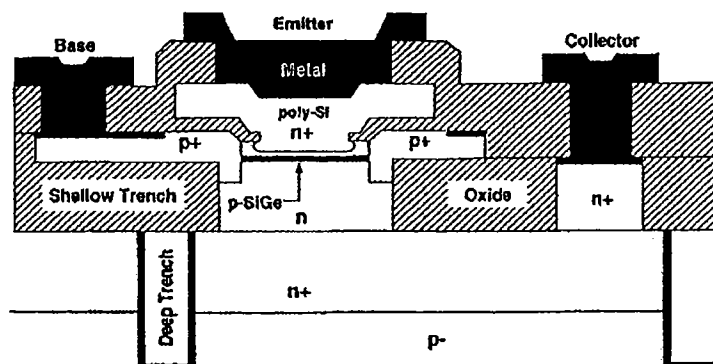
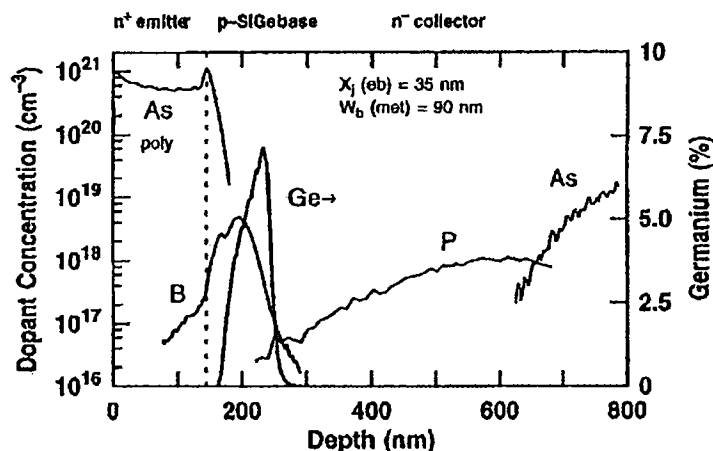Fig. 3. Schematic device cross section of a first-generation SiGe HBT.

Fig. 4. Representative first-generation SiGe HBT doping profile, as measured by SIMS.

with little or no process modification, providing compelling cost advantages.

Following this motivation, in Section III we briefly review the key elements of SiGe HBT technology, and in Section IV basic SiGe HBT device physics which have bearing on extreme environments. In Section V we address cryogenic temperature operation of SiGe HBTs, in Section VI the high-temperature operation of SiGe HBTs, and in Section VII the operation of SiGe HBTs in a radiation-rich environment. We conclude with some general observations and identify important "open" issues for future research.

III. SiGe HBT Technology

While the specific composition of a given SiGe HBT clearly depends on the technology-generation (first, second, or third generation), and obviously the company manufacturing it, a representative state-of-the-art SiGe HBT BiCMOS technology integrates multiple SiGe HBTs with different breakdown voltages, with very conventional silicon CMOS devices. Such SiGe HBT BiCMOS technologies are 100% silicon processing compatible, employ deep- and shallow-trench isolation, a polysilicon emitter contact, and

a carbon-doped (to decrease the boron diffusivity [9], [10]) graded epitaxial SiGe base which is thermodynamically stable as deposited, and typically grown by some variant of a chemical vapor deposition process (e.g., UHV/CVD or RTCVD). Such SiGe technologies are designed to be high yielding and manufacturable, and often achieve transistor chain yields (e.g., 5000 SiGe HBTs wired in parallel) in excess of 90%. Various commercial implementations of SiGe HBT technologies are given in [11]–[24].

Fig. 3 shows a schematic cross section of a first-generation SiGe HBT. Note the locations of the emitter-base spacer and shallow trench isolation (STI) regions. These two regions form the primary Si–oxide interfaces within easy reach of the main electron and hole current flows in the device and hence figure prominently in any discussion involving radiation effects, for instance.

A representative first-generation doping and Ge profile is shown in Fig. 4. In this case, the metallurgical base width is about 90 nm (about 65-nm neutral base width under forward-active bias), the metallurgical emitter junction depth is about 35 nm (from the Si surface), and the peak Ge content is about 8% (it is thermodynamically stable). The emitter polysilicon layer is doped to solid-solubility

limits, multiple self-aligned phosphorus implants are used to locally tailor the collector doping profile, and the peak base doping is about 4×10^{18} cm^{-3}. The Ge profile is trapezoidal in shape, with substantial grading across the neutral base. This vertical profile design can be considered quite conservative by today's standards, but it nonetheless achieves a peak f_T of 50 GHz (70-GHz peak f_{max}) at a BV_{CEO} of 3.3 V, solidly in the range of a first-generation technology. Cross-company typical profile numbers for first-generation SiGe technologies are $W_{b0} = 60-90$ nm, $W_c = 20-40$ nm, peak Ge = 8–12%. Representative second-generation technology achieves a peak f_T of 100–120 GHz (100–150-GHz peak f_{max}) at a BV_{CEO} of 2.0–2.4 V. Cross-company typical profile numbers for second-generation SiGe technologies are $W_{b0} = 40-60$ nm, $W_c = 20-40$ nm, peak Ge = 15–25%.

In third-generation SiGe technology, an improvement in f_T to 200 GHz (and above) is typically realized only through fundamental changes in the physical structure of this first-generation transistor. Specifically, a reduced thermal cycle "raised extrinsic base" structure is implemented using conventional deep and shallow trench isolation, and an *in situ* doped polysilicon emitter. The key features of this more advanced structure include: 1) a removal of any additional extrinsic base ion implantation, which generally produces an undesirable enhanced base dopant diffusion, and 2) the physical relocation of the extrinsic base-collector junction, making reduction of collector-base capacitance easier. The entire thermal cycle required to build the device is reduced.

Those acquainted with Si BJT technologies will recognize the similarity in doping profiles between this SiGe HBT and advanced ion-implanted Si BJTs (just removing the Ge makes it look like a high-speed Si BJT). The key difference between this SiGe HBT and a conventional ion-implanted double-poly Si BJT lies in the base profile, which can be much more heavily doped at a given base width using epitaxial growth (leading to much lower base resistance, better dynamic response, and lower noise).

Regardless of the SiGe growth technique used, the structure, the self-alignment scheme employed in fabricating the transistor, or technology generation, strained SiGe films found in today's commercially viable SiGe HBTs all have a similar form. The deposited SiGe film actually consists of a three-layer composite structure: 1) a thin, undoped Si buffer layer; 2) the actual boron-doped SiGe active layer; and 3) a thin, undoped Si cap layer. The Si buffer layer is used to start the growth process off on the right foot, and serves two purposes. First, the Si buffer layer helps to ensure that a pristine SiGe epitaxial growth interface is preserved between the original Si substrate, which was grown by a high-temperature Si epitaxy process, and the coming SiGe strained layer that will be grown by a more difficult low-temperature epitaxy process. Maintaining a contaminant-free growth interface with perfect crystallinity is essential for obtaining device-quality SiGe films. Second, this Si buffer layer also frequently plays a role in device design for extreme environments, since it allows the incorporation of intrinsic layers (i-layers) to be easily embedded in the collector-base junction and can be used to decrease

the junction field and aid in both breakdown voltage and parasitic junction leakage tailoring.

The active SiGe layer has a position-varying Ge composition, and an embedded boron-doping spike, typically deposited as a boron box profile for a given integrated base charge. The SiGe layer forms the active region of the bandgap-engineered device, and the specific shape, thickness, and placement of the Ge profile with respect to the boron base profile will in large measure determine the resultant dc and ac performance of the transistor.

Finally, the Si cap layer serves four purposes. First, it provides a Si termination to the SiGe composite. This is particularly important, since most SiGe HBT fabrication approaches involve some form of oxidation step to form the emitter-base spacer used in self-alignment, and SiGe does not oxidize well. Second, the Si cap provides additional space to allow the modest out-diffusion of the boron base profile during processing, while at the same time providing room for the emitter out-diffusion. Third, as with the Si buffer layer, a Si cap layer can be used to introduce an active i-layer into the emitter-base junction to lower the junction electric field and thereby reduce the parasitic EB tunneling current, which typically limits the base current ideality at low-injection and hence degrades device reliability. Finally, an unintentional but nonetheless important consequence of having this Si cap layer is that it helps improve the overall stability of the film, increasing the thickness and Ge fraction of the layer to levels higher than might otherwise be expected. The thickness of the SiGe-bearing layer is clearly a key variable in SiGe HBT device design for extreme environments. The maximum thickness for obtaining pseudo-morphic growth postfabrication (i.e., after any thermal anneals or ion-implantation steps which might relax an overstable film) is known as the "critical thickness," and the dependence of the SiGe film thickness on average Ge film content is known as the SiGe "stability constraint curve." Recent theoretical approaches [25] which properly account for effects of the Si cap layer on film stability show good agreement between stability calculations and data for real SiGe films used in practical SiGe HBTs. Representative SiGe stability constraint curves is shown in Fig. 5.

IV. SiGe HBT Device Physics

To fully appreciate many of the constraints faced in the operation of SiGe HBTs in extreme environments, particularly as a function of technology scaling, it is useful to have good picture of the physical operation of these devices, and particularly how their operation differs from a similarly constructed Si BJT. The introduction of Ge into the base region of a bipolar transistor has two tangible dc consequences and can best be appreciated by viewing an energy band diagram (Fig. 6).

1) The potential barrier to injection of electrons from emitter into the base is decreased. Intuitively, this will yield exponentially more electron injection for the same applied V_{BE}, translating into higher collector
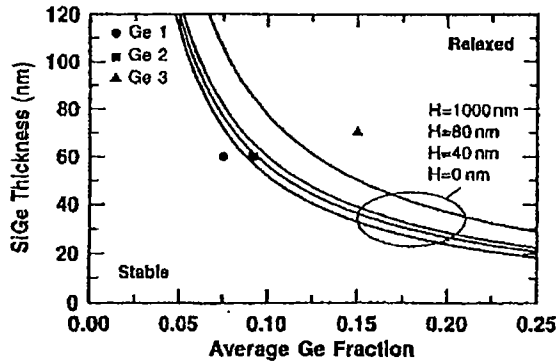
Fig. 5. Theoretical stability constraint curves as a function of average Ge fraction and Si "cap" thickness (H). Also shown are several representative SiGe profiles, two of which are thermodynamically stable, and one which is metastable and hence will relax during fabrication.
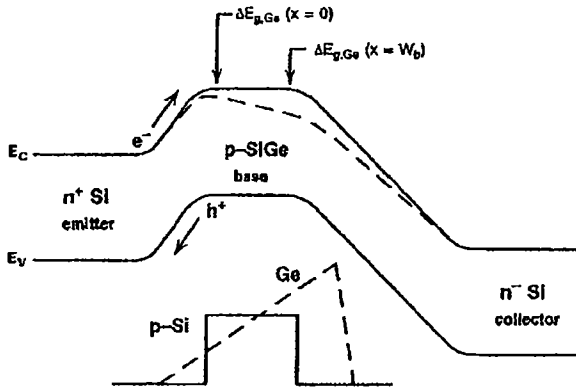

Fig. 6. Energy band diagram for a Si BJT and graded-base SiGe HBT, both biased in forward active mode at low injection.

current and hence higher current gain (β) in the device, provided the base current remains unchanged. Of great practical importance, the introduction of Ge effectively decouples the base doping from the current gain, thereby providing device engineers with much greater design flexibility than in Si BJTs.

2) The presence of a finite Ge content in the CB junction will positively influence the output conductance of the transistor, yielding higher Early voltage (V_A).

For an identically constructed (doping levels, layout, emitter contact, etc.) SiGe HBT and Si BJT, we find (for a detailed derivation of the following equations, refer to [1]):

$$\frac{\beta_{SiGe}}{\beta_{si}}\bigg|_{V_{BE}} \simeq \left\{ \frac{\tilde{\eta}\eta\Delta E_{g,Ge}(grade)}{kTe^{\Delta E_{g,Ge}(0)/kT}}{1 - e^{-\Delta E_{g,Ge}(grade)/kT}} \right\} \quad (1)$$

where we have defined a minority electron diffusivity ratio between SiGe and Si as

$$\eta = \frac{(D_{nb})_{SiGe}}{(D_{nb})_{Si}} \quad (2)$$

and an "effective density-of-states ratio" between SiGe and Si according to

$$\gamma = \frac{(N_C N_V)_{SiGe}}{(N_C N_V)_{Si}} < 1. \quad (3)$$

The Ge-induced reduction in the base bandgap occurring at the emitter-base edge of the quasi-neutral base is $\Delta E_{g,Ge}(x = 0)$, and

$$\Delta E_{g,Ge}(grade) = \Delta E_{g,Ge}(W_b) - \Delta E_{g,Ge}(0) \quad (4)$$

where W_b is the quasi-neutral base width. These Ge-induced band offsets can in fact be electrically inferred from device dc data [26].

The output conductance ratio (as reflected in the Early voltage) between a SiGe HBT and a Si BJT exponentially depends on the amount of bandgap grading across the base divided by kT

$$\frac{V_{A,SiGe}}{V_{A,Si}}\bigg|_{V_{BE}} \simeq e^{\Delta E_{g,Ge}(grade)/kT}\left[\frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\Delta E_{g,Ge}(grade)/kT}\right] \quad (5)$$

Combining (1) and (2) yields the key analog figure-of-merit (βV_A)

$$\frac{\beta V_{A,SiGe}}{\beta V_{A,Si}} = \gamma\tilde{\eta}\eta e^{\Delta E_{g,Ge}(0)/kT}e^{\Delta E_{g,Ge}(grade)/kT}. \quad (6)$$

To understand the dynamic response of the SiGe HBT, and the role Ge plays in transistor frequency response, we must first formally relate the changes in the base transit time and emitter transit time to the physical variables of this problem. The base transit time ratio, which typically limits the achievable frequency response ($f_T \propto 1/\tau_b$), is given by

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\eta}\frac{kT}{\Delta E_{g,Ge}(grade)} \cdot \left\{1 - \frac{kT}{\Delta E_{g,Ge}(grade)}\left[1 - e^{-\Delta E_{g,Ge}(grade)/kT}\right]\right\}. \quad (7)$$

The increase in current gain also has a favorable impact on the f_T of the transistor, since the emitter delay time can be a nonnegligible component of the overall emitter-to-collector delay ($\tau_e \propto 1/\beta$), such that

$$\frac{\tau_{e,SiGe}}{\tau_{e,Si}} \simeq \frac{J_{C,Si}}{J_{C,SiGe}} = \frac{1 - e^{-\Delta E_{g,Ge}(grade)/kT}}{\gamma\tilde{\eta}\frac{\Delta E_{g,Ge}(grade)}{kT}e^{\Delta E_{g,Ge}(0)/kT}}. \quad (8)$$

Both τ_b and τ_e couple to the overall unity-gain cutoff frequency (f_T) according to

$$f_T = \frac{1}{2\pi}\left[\frac{kT}{qI_C}(C_{te}+C_{tc})+\tau_b+\tau_e+\frac{W_{CB}}{2v_{sat}}+r_cC_{tc}\right]^{-1}. \quad (9)$$

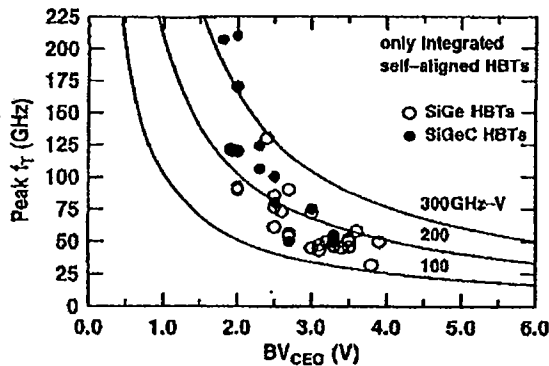These Ge-induced improvements in the base and emitter transit times, when coupled to a laterally scaled device

Fig. 7. Peak unity-gain cutoff frequency as a function of open-base collector-to-emitter breakdown voltage for self-aligned SiGe and SiGeC HBTs.

V. LOW-TEMPERATURE OPERATION

Bandgap engineering generally has a positive influence on the low-temperature characteristics of bipolar transistors [1]. SiGe HBTs operate very well, in fact, in the cryogenic environment (e.g., liquid nitrogen temperature = 77.3 K = −320 °F = −196 °C), an operational regime traditionally forbidden to Si BJTs. While the large power dissipation associated with conventional bipolar digital circuit families such as emitter coupled logic (ECL) would likely preclude their widespread use in cooling-constrained cryogenic systems, the combination of cooled, low-power, scaled Si CMOS with SiGe HBTs offering excellent frequency response, low noise performance, radiation hardness, and excellent analog properties represents a unique opportunity for the use of SiGe HBT BiCMOS technology in cryogenic systems.

A. Impact of Cooling on Bipolar Transistors

The detrimental effects of cooling on homojunction bipolar transistor operation have been appreciated for many years [31]–[35]. While the precise dependence of Si BJT properties on cooling can be a strong function of technology generation and profile design, Si BJT device and circuit properties cooled to cryogenic temperatures typically exhibit [36]–[41]:

- a modest increase (degradation) in the junction turn-on voltage with decreasing temperature (monotonic);
- a strong increase (improvement) in the low-injection transconductance with cooling (monotonic);
- a strong increase (degradation) in the base resistance with cooling (typically, quasi-exponential below about 200 K);
- a mild decrease (improvement) in parasitic transistor depletion capacitances (monotonic);
- a strong decrease (degradation) in β with cooling (quasi-exponential);
- a modest decrease (degradation) in frequency response with cooling, with f_T typically degrading more rapidly than f_{max} with decreasing temperature (monotonic below about 200 K);
- an increase (degradation) in ECL circuit delay with cooling (monotonic below about 200 K);
- the noise margin of current-switch-based digital circuits (e.g., ECL) increases (improves) with cooling (monotonic), allowing reduced logic swing operation.

The impact of cooling of Si BJTs is typically largely one of serious device and circuit performance degradation, effectively precluding their use in cryogenic applications. As will be seen, the addition of SiGe to this low-temperature problem can be used to change this situation dramatically.

B. Cryogenic Operation of SiGe HBTs

Intuitively, we expect that band-edge effects induced by bandgap engineering will generally couple strongly to bipolar transistor properties. This strong coupling is physically the consequence of the fact that the bipolar transistor is a minority carrier device, and hence the terminal currents are proportional to n_{i0}^2 via the Shockley boundary conditions,

structure, translate into significant improvements in the maximum oscillation frequency (f_{max}) of the SiGe HBT as well, which is a more relevant figure of merit for most mixed-signal circuit applications. It is important to note that with technology scaling, the average collector current density at which peak f_T (or f_{max}) occurs increases rapidly. For a typical first-generation (50-GHz) SiGe HBT, peak f_T might be at J_C = 1–2 mA/μm^2, whereas it might be 8–10 mA/μm^2 for second-generation (120-GHz) technology, and 15–20 mA/μm^2 for third-generation (200-GHz) technology. This increase in operating current density is the result of the need to delay the onset of both Kirk effect (base push-out) and high-injection heterojunction barrier effects [27], [28], which, if unchecked, will quickly limit the maximum performance attainable. Note, however, that this increase in current density is usually obtained at a overall decrease in operating current, since lateral scaling produces smaller emitter geometries, and thus thermal effects (driven by I_C and not J_C) do not necessarily worsen with scaling.

An unfortunate consequence of optimizing SiGe HBTs for higher peak f_T (via higher collector doping) is a strong increase in impact-ionization in the base-collector space-charge region. Thus, an inherent (and well known) tradeoff exists between peak f_T and BV_{CEO} in SiGe HBT device design, often referred to as the Johnson limit (Fig. 7) [29]. This Johnson limit, however, is actually more accurately described by the (larger) $BV_{CES}f_T$ product (BV_{CES} is about equal to BV_{CBO}) than the traditional $BV_{CEO}f_T$ product [30], but clearly the ever-decreasing operational voltage limits of scaled SiGe HBTs pose important (and often nonobvious) constraints on the biasing and operation of SiGe HBTs used in mixed-signal circuits. The understanding, for instance, of how much "usable" voltage actually exists in the region between BV_{CEO} and BV_{CES} remains an active research topic, particularly when considering the complex interactions in breakdown between impact-ionization, self-heating, and avalanche-induced, current-crowding instabilities (often referred to as pinch-in effects), and their corresponding dependence on operational current density. These issues have potentially important implications for use of SiGe HBTs in extreme environments.
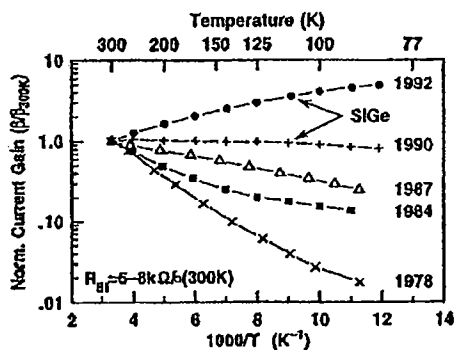
Fig. 8. Evolution of current gain temperature dependence with Si-based bipolar technology generation. The last two generations are SiGe HBT technologies.

Fig. 9. Evolution of unloaded ECL gate delay at 310 K and 84 K with Si-based bipolar technology generation. The last two generations are SiGe HBT technologies.

with n_{i0}^2 being in turn proportional to the exponential of the bandgap. Hence, changes to the bandgap will couple exponentially to the currents. Furthermore, from very general statistical mechanical considerations, these bandgap changes will inevitably be divided by the thermal energy (kT), such that a reduction in temperature will greatly magnify any bandgap changes. Not surprisingly, then, even a cursory examination of the SiGe HBT device equations suggests that both the dc and ac properties of SiGe HBTs should be favorably affected by cooling [42], [43]. In fact, the thermal energy (kT), *in every instance*, is arranged in the SiGe HBT equations such that it favorably affects the low-temperature properties of the particular performance metric in question, be it $\beta(T)$, $f_T(T)$, or $V_A(T)$.

The beneficial role of temperature in SiGe HBTs can be used to easily offset the inherent bandgap narrowing induced degradation in current gain of a Si BJT to achieve viable dc operation down to 77 K, even for a SiGe HBT that has not been optimized for the cryogenic environment. Fig. 8 shows the evolution of peak current gain as a function of reciprocal temperature from early Si BJT technologies circa 1978 to SiGe technologies circa 1992. Clearly, the addition of Ge-induced bandgap engineering enables functional current gain down at least to 77 K with minimal effort. From a dynamic point of view, the Ge-grading-induced base drift field provides a means to offset the inherent r_b degradation associated with cooled Si BJTs, yielding an f_T that does not degrade with cooling. Since the reduced thermal cycle nature of epitaxial growth techniques are generally more conducive to maintaining thinner, more heavily doped base profiles than conventional ion-implanted bases used in modern Si BJTs, it is fairly straightforward to control base freeze-out in SiGe HBTs, at least down to 77 K, and hence R_b at cryogenic temperatures can be more easily controlled. If f_T and R_b do not degrade significantly with cooling, then achieving respectable circuit performance down to 77 K becomes a reality unknown to Si BJT technologies.

Fig. 9 shows the evolution of unloaded ECL gate delay as a function of publication date. As expected, optimized 300 K technology scaling successfully improved circuit speed over time. More surprising, perhaps, is that the rate
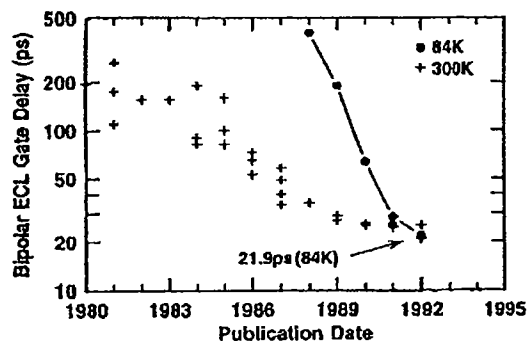
of improvement in low-temperature performance was significantly faster. The 1991 and 1992 cryogenic data points are for SiGe HBT technologies and clearly demonstrate that one can no longer out of hand dismiss Si-based bipolar technologies for the cryogenic applications. SiGe can thus be viewed as an effective means to extend Si-based bipolar technology to the cryogenic environment (with little or no effort). This scenario is particularly appealing if we consider state-of-the-art SiGe HBT BiCMOS technologies, since Si CMOS also performs well down to 77 K, and provides a major advantage in the reduction in power dissipation, an often serious constraint given the limited efficiency of cryocoolers. While it is unlikely that one would develop SiGe technology explicitly for cryogenic applications, if (as is the case), one could simply take a room temperature-optimized SiGe technology and operate it at low temperatures without serious modification, that prospect might prove cost effective. With the present trend toward reduced-temperature operation of CMOS-based high-end servers as a performance and reliability enhancement vehicle (currently at 0 °C to −40°C and going lower), the appeal of SiGe HBT BiCMOS technologies for the cryogenic environment may naturally grow over time, since HBTs can provide numerous advantages over CMOS in analog, RF, heavily loaded digital, and high-speed driver/receiver applications.

We first examine the expected theoretical temperature dependence of the important SiGe HBT performance metrics. Compared to a comparably constructed Si BJT, $\beta(T)$ (1) in a SiGe HBT should increase exponentially with decreasing temperature (Fig. 10). In addition, $V_A(T)$ and $\beta V_A(T)$ in a SiGe HBT should also increase exponentially with decreasing temperature compared to a comparably constructed Si BJT [(5),(6)] and is again confirmed experimentally (Fig. 11).

The anticipated temperature dependence of the frequency response of a SiGe HBT can be gleaned from the temperature dependence of the base and emitter transit times [(7)–(9)]. Both are favorably influenced by cooling, and thus we expect that the influence of the graded SiGe base is sufficient to overcome the inherent electron diffusivity degradation on r_b with cooling, and this is indeed the case experimentally.
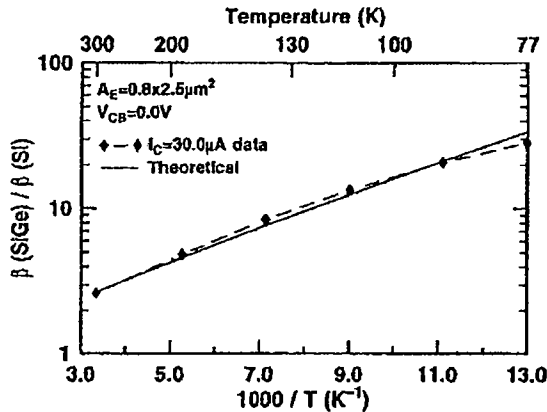
Fig. 10. Measured and calculated current gain ratio as a function of reciprocal temperature for a comparably constructed SiGe HBT and Si BJT.
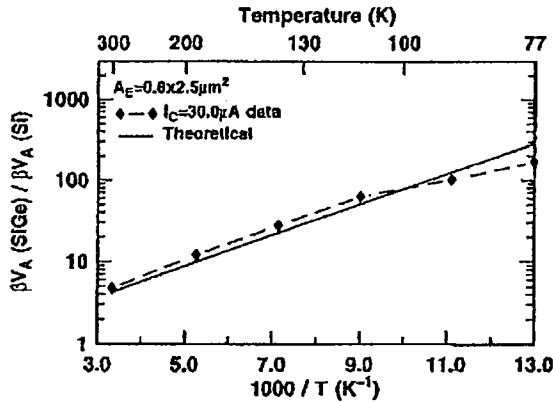

Fig. 11. Measured and calculated ratio of the current gain–Early voltage product ratio as a function of reciprocal temperature for a comparably doped SiGe HBT and Si BJT.

C. Low-Temperature Design Constraints

While SiGe HBTs designed for room temperature operation generally function acceptably well down to 77 K, second-order design constraints do, nonetheless, exist and can impact profile optimization [44], [45]. The first such constraint centers on the base current and its impact on the current gain at low injection. While conventional Shockley–Read–Hall (SRH) recombination exponentially decreases with cooling, thereby effectively eliminating reverse leakage in the collector-base junction, the same is not true of carrier tunneling processes, whether they are band-to-band or trap-assisted. Given that the EB junction of high-speed bipolar transistors (either Si or SiGe) are typically quite heavily doped (often in the vicinity of 1×10^{18} cm^{-3}), the doping induced electric field is high and can result in substantial parasitic tunneling leakage. While this is generally easily designed around in 300 K designs, it is more problematic at low temperatures, given that the collector and base currents decrease strongly at fixed V_{BE} as the temperature drops. In this case, as the

base current decreases with cooling, any tunneling-induced leakage will remain roughly constant, hence uncovering a parasitic leakage "foot" on the base current. This parasitic base leakage current can severely limit the current gain at low injection at cryogenic temperatures. Thus, as a rule of thumb, it can be safely stated that the ideality of the base current of a high-performance Si or SiGe bipolar transistor will never improve with cooling. If the base current is ideal (i.e., $e^{qV_{BE}/kT}$) down to a picoamp at 300 K, it may be ideal only to a nanoamp at 77 K. If it is even modestly nonideal at 300 K, it will be quite leaky at 77 K. How serious a limitation this leakage is depends strongly on the circuit application. In digital logic, for instance, it is not an issue, given that the devices are biased well out of the leakage regime, and β does not strongly couple to circuit speed. For more sensitive analog circuits, however, it can in principle require careful design consideration. As discussed below, one can optimize a SiGe HBT to reduce this leakage effect, a feat much more easily accomplished using epitaxial growth rather than ion implantation for the base layer formation.

More worrisome than the base current at low temperatures, however, is the enhancement of high-injection, heterojunction barrier effects with cooling. Band-edge effects in bipolar transistors generally couple very strongly to the device properties, and barrier effects are no exception. In this case, given that barrier effects necessarily exist in all practical SiGe HBTs, cooling will make the situation decidedly worse. The consequences of barrier effects, as at room temperature, include a premature rolloff in both β and f_T at high J_C and place a limitation on maximum output current drive. What is different in the context of cryogenic operation, however, is that while a well-designed 300 K SiGe HBT may not show any clear evidence of barrier effect at 300 K, it will certainly show evidence of it at 77 K, and its impact on device performance will be correspondingly worse. That is, the design margin for 77 K operation is in essence narrower, always an undesirable situation. The device transconductance is a useful tool for assessing barrier effects in SiGe HBTs. A comparison of g_m between comparably designed i-p-i SiGe HBTs and i-p-i Si BJTs clearly shows that while g_m at low J_C increases with cooling as expected, a dramatic drop in g_m at a higher critical current density close to that of Kirk effect can be observed in the SiGe HBT. Fortunately, it is also true that this critical onset current density in fact increases with cooling, consistent with the fact that the saturation velocity rises at low temperatures, thus delaying Kirk effect until higher J_C. As discussed below, this result can be traded off to optimize SiGe HBTs for 77 K operation. One would also expect that barrier effect would have a serious impact on transistor dynamic response, given that enhanced charge storage in the base couples strongly to f_T.

D. Optimization of SiGe HBTs for 77 K

While conventional 300 K SiGe HBT designs will inherently function reasonably well down to 77 K, it remains to be seen whether a SiGe HBT designed *specifically* for 77 K operation can achieve significantly better device and circuit

performance at 77 K than it has at 300 K, and what the design issues and tradeoffs faced in achieving this goal would be.

To address the explicit optimization of a SiGe HBT for 77 K operation, a new profile design point and fabrication scheme is required [46]. In this case, an epitaxial "emitter-cap" layer doped with phosphorus at about 1×10^{18} cm^{-3} was deposited *in situ* in a UHV/CVD deposition tool on top of the SiGe-base to form the EB junction. This 77 K optimized SiGe HBT will be referred to as an epitaxial "emitter-cap" SiGe HBT [47]. Because EB carrier tunneling processes depend exponentially on the peak junction field, the lightly doped emitter is expected to minimize the parasitic EB tunneling current compared to a conventional "i-p-i" SiGe HBT design. In addition, the increase in carrier saturation velocity with cooling, as well as the presence of velocity overshoot in the CB space-charge region at 77 K, results in an onset current density of base push-out (Kirk effect) that is about 50% larger at 77 K than at 300 K [44]. Thus, compared to a 300 K design, the collector doping level can be decreased in an optimized 77 K profile. In this case, the doping level at the metallurgical CB junction was lowered from 1×10^{17} cm^{-3} for the conventional SiGe HBT design to about 2×10^{16} cm^{-3} and ramped upward toward the subcollector to minimize freeze-out deep in the neutral collector. This 77 K collector profile is used to reduce the parasitic CB capacitance under the constraint that the onset current density of the SiGe–Si heterojunction barrier be above the maximum operating current density of about 1.0 mA/μm^2.

To ensure a low emitter resistance, a 200-nm *in situ* doped polysilicon contact was deposited on top of the composite EB profile (n-cap/p-SiGe). Because the arsenic out-diffusion from the heavily doped polysilicon layer is used only to contact the epitaxial phosphorus emitter and does not determine the metallurgical EB junction, only a very short rapid thermal annealing (RTA) step is required to activate and redistribute the emitter dopants, allowing the maintenance of a thin, heavily doped base. A metallurgical emitter-cap thickness of about 10 nm was achieved at the end of processing (estimated by subtracting the arsenic out-diffusion of the emitter poly from the total EB junction depth). The boron doping of the base profile was increased over a more conventional i-p-i SiGe design to improve its base freeze-out properties, and was deposited as a box 10 nm wide by 2.5×10^{19} cm^{-3}. At the end of processing the metallurgical base was about 75 nm wide with a peak concentration of about 8×10^{18} cm^{-3}, well above the Mott transition for carrier freeze-out. To minimize minority carrier charge storage in the emitter-cap layer, a large 77 K β is also desirable ($\tau_c \propto 1/\beta_{ac}$). Therefore, a trapezoidal Ge profile with 3%–4% Ge at the EB junction (compared to about 0%–1% for the standard design) and ramping to 8.5% at the CB junction (compared to about 8.5% for the standard design) was used. The resultant emitter-cap Ge profile was about 65 nm thick, and satisfied the thermodynamic stability criteria for UHV/CVD blanket films.

This 77 K SiGe design point yields a transistor with reasonably ideal Gummel characteristics at low temper-
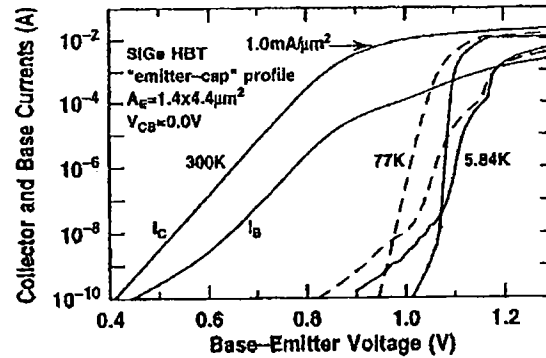

Fig. 12. Gummel characteristics at 300 K, 77 K, and 5.84 K for a 77 K optimized emitter-cap SiGe HBT.
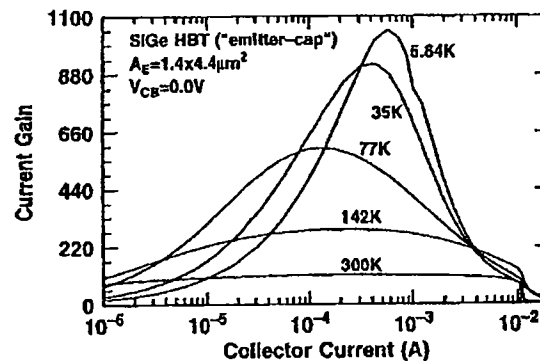

Fig. 13. Current gain versus bias current as a function of temperature for a 77 K optimized emitter-cap SiGe HBT.

atures, with a maximum output current drive well above 1.0 mA/μm^2 at 84 K (Fig. 12). The higher Ge concentration at the EB junction, the beneficial effects of the emitter high–low (n^+/n^- cap) junction, and the bandgap narrowing of the heavily doped base, offset the bandgap narrowing of the heavily doped emitter region to yield a peak β that increases quasi-exponentially with cooling from 102 at 310 K to 498 at 84 K (Fig. 13). This large β value at low temperatures serves to minimize the unwanted charge storage associated with the emitter-cap layer as well as to circumvent the degradation of β at medium injection levels due to bias-dependent Ge ramp effects, giving an ideal value of β of 99 at 84 K at a typical circuit operating point of 1.0-mA collector current [47]. An undesirable result of the high β at low temperature, however, is a decrease in the BV_{CEO} from 3.1 V at 310 K to 2.3 V at 84 K, but it remains acceptable for most circuit applications. Depending on circuit requirements at 77 K, the low-temperature current gain can be easily tuned to a desired value.

The reduction in overall thermal cycle compared to a conventional design is key to maintaining the abrupt, as-deposited boron base profile, and thus providing immunity to carrier freeze-out at cryogenic temperatures (R_{bi} only increases from 7.7 to 11.0 kΩ/□ between 310 K and 84 K).
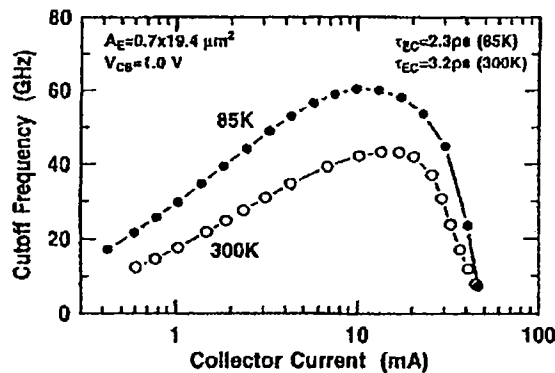
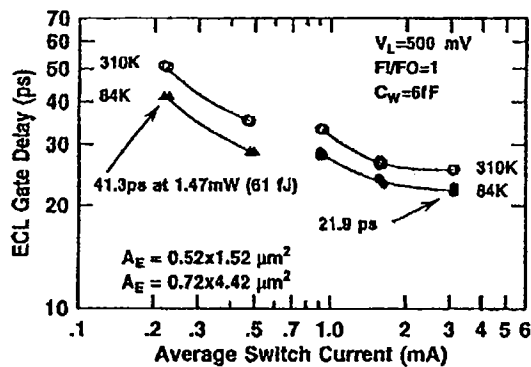Fig. 14. Cutoff frequency characteristics at 300 K and 77 K for a 77 K optimized emitter-cap SiGe HBT.

Fig. 15. Unloaded ECL gate delay as a function of power at 310 K and 84 K.

Importantly, this immunity to base freeze-out does not come at the expense of increased EB leakage, as it does, for instance, in a spacer-free SiGe profile with a very heavily doped base [44]. The lower doping level of the emitter-cap layer results in a reverse EB leakage at 1.0 V at 84 K, which is more than 500 times smaller than for the conventional SiGe design. The consequence is a much smaller forward tunneling component in the base current (much larger low-current β), a smaller EB capacitance, and an expected improvement in hot-carrier reliability at cryogenic temperatures.

As shown in Fig. 14, the transistor cutoff frequency (f_T) rises from 43 GHz to 61 GHz with cooling to 85 K due to the beneficial effects of the Ge-grading-induced drift field. This improvement in f_T, coupled to the low total base resistance and slightly decreased CB capacitance, yields an increase in maximum oscillation frequency with cooling as well, from 40 GHz at 310 K to 50 GHz at 84 K. To assess the 77 K circuit capabilities of this technology, unloaded ECL ring oscillators were measured (Fig. 15). High-power (12.45-mW) ECL circuits switch at a record 21.9 ps at 84 K, 3.5 ps faster than at 310 K. Circuits that were optimized for lower power operation achieve a minimum power-delay product of 61 fJ (41.3 ps at 1.47 mW) at 84 K, and are 9.6 ps faster than
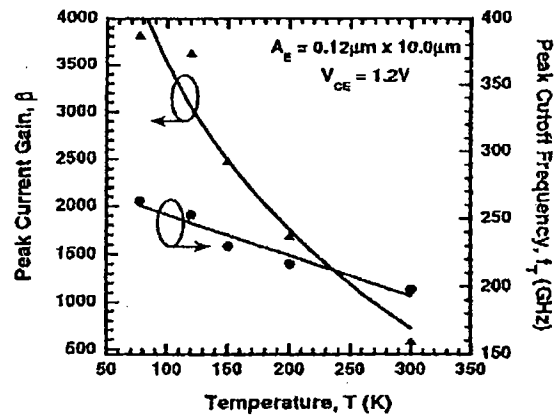

Fig. 16. Current gain and peak cutoff frequency as a function of temperature for an nonoptimized third-generation SiGe HBT.

at 310 K. These 77 K optimized ECL circuits are expected to exhibit even more dramatic improvements in speed over room-temperature ECL circuits under heavy loading, due to the beneficial effects of cooling on metal interconnect resistance and circuit logic swing [45]. The delay improvement at long interconnect wire lengths can be dramatic (2.7 × faster at 84 K than at 300 K at 10-mm wire length), and suggests that SiGe HBT based line-drivers might be attractive for 77 K applications.

Recent measurements on noncryogenically optimized 200-GHz, third-generation SiGe HBTs, show even more impressive performance down to liquid nitrogen temperature [48], [49] (refer to [50], [51] for recent cryogenic results on a different third-generation SiGe technology). Current–voltage measurements across the 300 K to 85 K temperature range were made on SiGe HBTs with an emitter area of 0.12×10.0 μm^2. In spite of the high peak base and emitter doping levels associated with these aggressively scaled SiGe HBTs ($> 10^{19}$ cm^{-3}), the base current remains reasonably ideal at 85 K. This is the result of the lightly doped epitaxial spacer layer inserted between the base and emitter regions and helps limit field-assisted tunneling and recombination at low temperatures. The base and emitter regions in this device are both doped above the Mott transition and ensure that carrier freeze-out does not negatively impact the base or emitter resistance below 100 K. This device is capable of very high current density operation (>25 mA/μm^2), and thus the high collector doping level effectively limits the impact of heterojunction barrier effects at low temperatures. The current gain increases monotonically with cooling, from 600 at 300 K to 3800 at 85 K (Fig. 16). Two mechanisms are responsible for this improvement with cooling: 1) the (sizable) Ge-induced band offset in this device (exponentially) increases the current gain with cooling and 2) the heavily doped base region partially offsets the doping-induced bandgap narrowing associated with the emitter region. There is a strong decrease in the current gain above its peak value at 85 K associated with the Ge-grading effect, but the current gain remains above 2000 at 85 K at
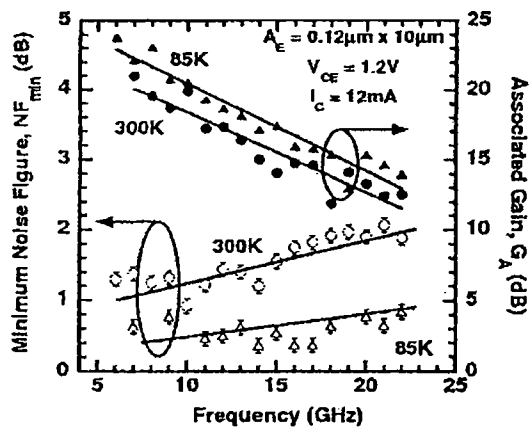
Fig. 17. Noise figure and associated gain as a function of temperature for an nonoptimized third-generation SiGe HBT.

the current density at which peak f_T is reached, effectively minimizing any emitter charge storage at low temperatures.

Fig. 16 also shows the shows the extracted peak cutoff frequency versus temperature for the $0.12 \times 10.0 \ \mu m^2$ SiGe HBT. An increase in peak f_T from 200 GHz at 300 K to 260 GHz at 85 K is observed. This increase in the peak f_T with cooling is proportionately smaller than has been reported in first-generation SiGe HBTs operated at 85 K. This is because in the present case, the base and emitter transit times in this 200-GHz device, which are favorably affected by both the Ge-grading and cooling, are already small compared to the collector delay time, and thus their relative influence on the total transit time with cooling is smaller. The extrapolated total emitter-to-collector delay decreases from 0.7 ps at 300 K to 0.6 ps at 150 K and 0.5 ps at 85 K, and the total depletion capacitance of the device decreases with cooling, as expected, since the junction built-in voltages increase with cooling.

Fig. 17 shows the the measured minimum noise figure (NF_{min}) and associated gain (G_{assoc}) as a function of frequency at $I_C = 12$ mA (i.e., at peak f_T), for a $0.12 \times 10.0 \ \mu m^2$ SiGe HBT, at both 300 K and 85 K. At 85 K, this device achieves a minimum NF_{min} of about 0.3 dB (with $G_{assoc} = 18$ dB) at 14 GHz, and a minimum NF_{min} of about 0.75 dB $(G_{Assoc} = 16$ dB) at 20 GHz, record numbers for SiGe HBTs operating at cryogenic temperatures.

E. Helium Temperature Operation

Long-wavelength infrared focal plane arrays (FPAs) and certain ultralow-noise instrumentation amplifiers require transistors that operate down to liquid helium temperature $(LHeT = 4.3$ K). In addition to evaluating SiGe HBT performance at these potential application temperatures, the below 77 K regime is ideally suited for investigating new device physics phenomena, as well as for testing the validity of conventional theoretical formulations of device operation (e.g., drift-diffusion). This is particularly true for a SiGe

HBT, since many of the transistor parameters are thermally activated functions of the Ge-induced band offsets, and are expected to change dramatically between 77 K and 4 K. For instance, a simple calculation of the intrinsic carrier density, to which the terminal currents are proportional, shows that a n_{io} changes by a factor of e^{3056} between 77 K and 4 K. Initial results on (unoptimized) Si BJTs to 10 K [52] showed transistor functionality but poor performance in the LHeT regime $(< 10$ K–15 K). More recent work [53] on SiGe HBTs optimized for 77 K operation showed more impressive performance results as well as revealed interesting new device physics effects.

The emitter-cap SiGe HBT optimized explicitly for 77 K achieved a β of 500, f_T of 61 GHz, f_{max} of 50 GHz, and a minimum ECL gate delay of 21.9 ps at 84 K. In cooling this transistor from 77 K to LHeT, the current gain increases monotonically from 110 at 300 K to 1045 at 5.84 K, although parasitic base current leakage limits the useful operating current to above about 1.0 μA at 5.84 K. Fig. 12 shows the Gummel characteristics of a $1.4 \times 4.4 \ \mu m^2$ emitter-cap SiGe HBT down to 5.84 K, and Fig. 13 shows the current gain as a function of bias current down to 5.84 K.

The severity of the base current leakage at low injection, and the Ge-ramp effect at medium injection, limits the current range where one obtains the peak current gain. The aggressive base profile design in the emitter-cap SiGe HBT design (peak N_{ab}^- close to 8×10^{18} cm^{-3}) leads to an R_{bi} of < 18 k$\Omega/\square$ at 5.84 K, much lower than a more conventional SiGe HBT design. Base freeze-out below 77 K depends very strongly on peak base doping and must be carefully optimized for LHeT applications. At temperatures as low as 5.84 K, this transistor has a maximum current drive in excess of 1.5 mA/μm^2 (limited by quasi-saturation and heterojunction barrier effects), with a peak transconductance of 190 mS. Theoretical calculations based on measured SIMS data were compared to the experimentally observed variation of peak current gain with temperature. Above 77 K, the temperature variation of peak current gain for the SiGe HBT is close to that theoretically expected, while at temperatures below 77 K, the exponential increase in current gain is primarily limited by parasitic base leakage due to field-enhanced tunneling. In contrast to this strong enhancement of current gain with cooling for the SiGe HBT, the current gain in a Si BJT fabricated with a comparable doping profile is significantly degraded at low temperatures, due to the strong bandgap narrowing in the emitter. A comprehensive discussion of other unique cryogenic phenomena in SiGe HBTs operating in the LHeT environment is presented in [1].

F. Unique Cryogenic Phenomena

Recent measurements of highly scaled 350-GHz SiGe HBTs in the cryogenic temperature range has led to observations of highly unusual device behavior, including a new, hysteretic, negative-differential-resistance (NDR) effect which is observed in the forced-I_B output characteristics (Fig. 18) [54]. This behavior is similar to the "hysteresis" $I-V$
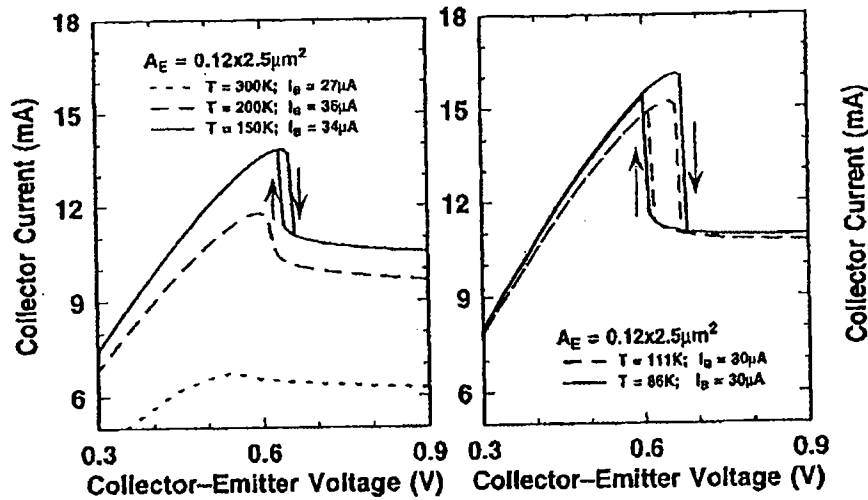
Fig. 18. Measured forced-I_B output characteristics of 350-GHz SiGe HBTs at different temperatures.

characteristics found in resonant tunneling diodes (RTD), but is of a different physical origin. The NDR disappears at low-injection levels (about 1/10 of the peak-f_T current density), indicating that the phenomenon is a high-injection effect, and comparisons to earlier generations of SiGe HBTs clearly indicates it is associated with vertical profile scaling. The observed NDR effect, along with the observed "hysteresis," are shown to be driven by the nonideal base current behavior as a function of V_{BE} and V_{CB}. These effects have been systematically investigated using different bias conditions, variable temperature operation, and various SiGe device generations. To explain and characterize the underlying physical mechanism and the consequent relation among the observations, we have presented an advanced SRH recombination model including trap-assisted tunneling. Calibrated one-dimensional (1-D) MEDICI simulations and analytical calculations were then used to support our explanations, as contained in [55].

VI. HIGH-TEMPERATURE OPERATION

While it has been demonstrated that SiGe HBTs operate well down to cryogenic temperatures, there was historically early concern about their suitability for operation at elevated temperatures. Given the narrow bandgap base region of the SiGe HBT compared to a Si BJT, and hence the expected negative temperature coefficient of the current gain (i.e., β decreases as temperature increases), it is often asked whether practical SiGe HBTs would have acceptable values of β at required high-end mil-spec operational temperatures (e.g., 125 °C). That this issue is not a valid concern for circuit designers is clearly demonstrated in Fig. 19, which compares the percent change in peak current gain between 25 °C and 125 °C for a Si BJT and a number or commercially relevant SiGe profiles. There are several important points to glean from these data.
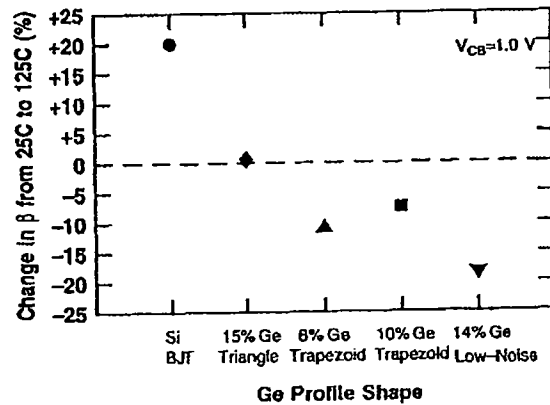

Fig. 19. Percent change in peak current gain between 25 °C and 125 °C for various Ge profiles.

- The current gain in SiGe HBTs does indeed have an opposite temperature dependence from that of a Si BJT, as expected from simple theory.
- These changes in β between 25 °C and 125 °C, however, are modest at best ($< 25\%$) and clearly are not cause for alarm for any realistic circuit.
- The negative temperature coefficient of β in SiGe HBTs is *tunable*, meaning that its temperature behavior between, say, 25 °C and 125 °C can be trivially adjusted to its desired value by changing the Ge profile shape near the EB junction. In the case of the 15% Ge triangle profile, with 0% Ge at the EB junction, β is in fact temperature independent from 25 °C to 125 °C. This points to a major advantage of bandgap engineering.
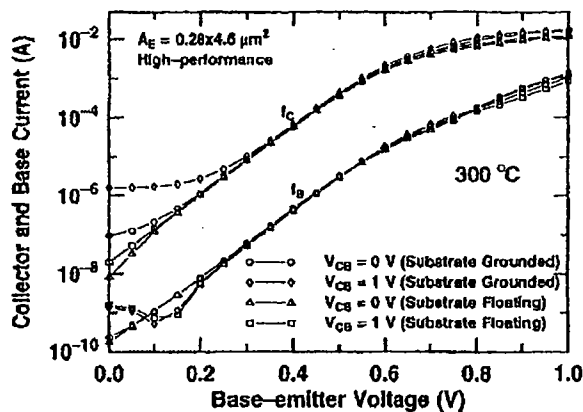
Fig. 20. Gummel characteristics at 300 °C with both floating and grounded substrate conditions.

Fig. 21. Current gain as a function of collector current at 25 °C, 150 °C, and 300 °C.

- Finally, it is well known that thermal-runaway in high-power Si BJTs is the result of the positive temperature coefficient of β (i.e., as the device heats up due to power dissipation, one gets more bias current, since the β increases with temperature, leading to a positive feedback process, and hence thermal collapse). The fact that SiGe HBTs naturally have a negative temperature coefficient for β suggests that this might present interesting opportunities for power amplifiers, since emitter ballasting resistors (which degrade RF gain) could in principle be eliminated, or at least reduced in value.

While the message that SiGe HBTs work just fine to 125 °C has at present generally been accepted, the applicability of SiGe HBTs to emerging extreme environment applications at considerably higher temperatures (say to 300 °C), has only very recently begun to be seriously contemplated. At present, the device technologies deployed for such high-temperature applications typically include SOI CMOS, GaAs, SiC, and GaN, all of which are expensive, and in some cases immature (i.e., SiC and GaN). Conventional Si CMOS and Si BJTs are typically limited to about 125 °C operation due to substrate leakage and reliability concerns, unless extensive (costly) modification to the device technologies is performed (e.g., adding SOI). The initial results on SiGe HBTs for high temperatures, however, are very encouraging [57], [58].

A. DC Characteristics

The Gummel characteristics of a state-of-the-art second-generation SiGe HBT at 300 °C is shown in Fig. 20. The turn-on voltage decreases as the temperatures increases, as expected, due to the decrease in the emitter-base built-in potential, and is driven by the changes in the intrinsic carrier density. Observe, however, that the device remains quite ideal at 300 °C, with a current gain above 100 and higher current drive capability than at room temperature, suggesting that the impact of high temperatures on the carrier mobility and hence
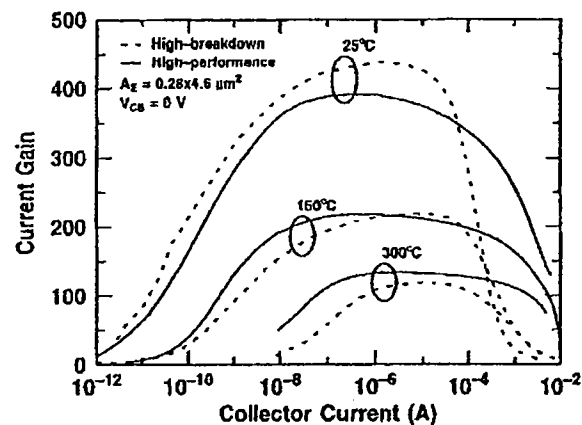
series resistances is not a serious factor. Clearly, minority carrier generation in the collector–substrate junction, and the consequent parasitic leakage, is a concern for high-temperature applications. The collector–substrate junction leakage current is generally dominated by space-charge region generation–recombination (G/R) leakage ($I_{gen} \propto n_i(T)$) over the range 25 to T_{tran}°C and by band-to-band thermal generation ($I_{diff} \propto n_i^2(T)$) above T_{tran}°C [59]. The collector–substrate leakage at 25 °C is less than the smallest detectable current of the measurement system (< 1 pA) and hence negligible in practical circuit applications. It can be seen from Fig. 20 that T_{tran}°C is about 135 °C for this SiGe technology. Fig. 20 shows the explicit impact of substrate leakage on the Gummel characteristics at 300 °C under bias. Observe that while the off-state leakage is 1.6 μA at 300 °C at $V_{CB} = 1$ V, and might be of potential concern for certain analog circuits biased at very low currents for high g_m, there remains over four orders of magnitude of useful bias range in this device at 300 °C.

The current gain as a function of collector current at 25 °C, 150 °C, and 300 °C for both the high-performance and the high-breakdown transistors is shown in Fig. 21. The shapes of the β versus I_C for high-performance and high-breakdown SiGe HBTs are profoundly different at high I_C. β for high-breakdown devices decreases rapidly at I_C close to 1 mA due to Kirk effect and heterojunction barrier effects (HBE) [28]. The higher collector doping level in the high-performance SiGe HBTs delays the onset of Kirk effect and hence HBE. Observe that with the increase of temperature, the HBE effect in high-breakdown HBTs becomes less important, due to the thermally activated nature of HBE [44]. This fact can provide additional design freedom regarding Kirk effect/HBE at high temperatures compared to at room temperature, which is clearly good news for high-temperature applications. Fig. 21 shows that the peak β decreases as temperature increases, as expected.

The transistor output characteristics remain ideal at temperatures up to 300 °C. The small negative slope in the output characteristics reflects self-heating in the device (Fig. 22).
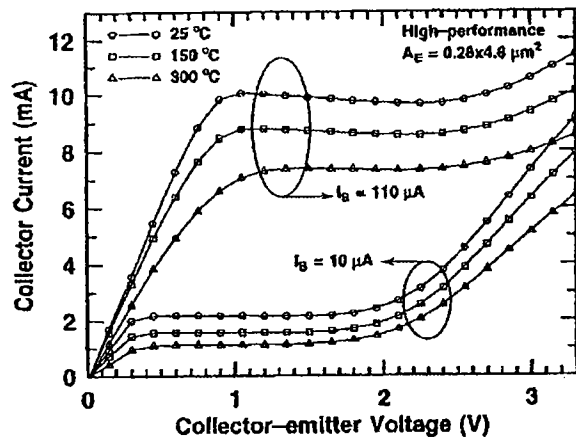
Fig. 22. f_T and f_{max} versus collector current density for a high-performance SiGe HBT.
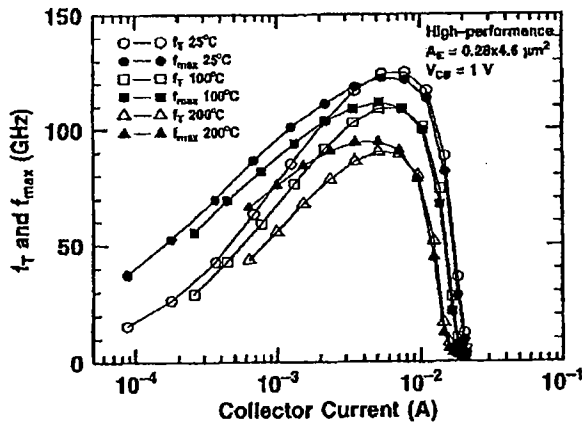

Fig. 23. f_T and f_{max} versus collector current density for a high-performance SiGe HBT.

B. AC Characteristics

The measured f_T and f_{max} versus bias current at 25 °C, 100 °C, and 200 °C are shown in Fig. 23 for the SiGe HBT. The peak f_T for the high-performance HBTs decreased by 29% across the temperature range, from 125 GHz at 25 °C to 89 GHz at 200 °C, while the peak f_{max} decreases by 23%, from 122 GHz at 25 °C to 94 GHz at 200 °C. The estimated peak f_T at 300 °C (beyond the measurement temperature range of our present test system) is about 75 GHz, clearly adequate for a large class of circuit applications.

C. Breakdown Voltage

Due to the finite impedance at the base terminal in real circuits, BV_{CEO} does not represent the maximum voltage that can be sustained on the device during circuit operation. From a temperature perspective, it does, however, provide an accurate gauge to the impact of high temperatures on the voltage limits for circuit design. The BV_{CEO} is to first order determined by the product of the M-1 and β at any given temperature. As β decreases with the increase of
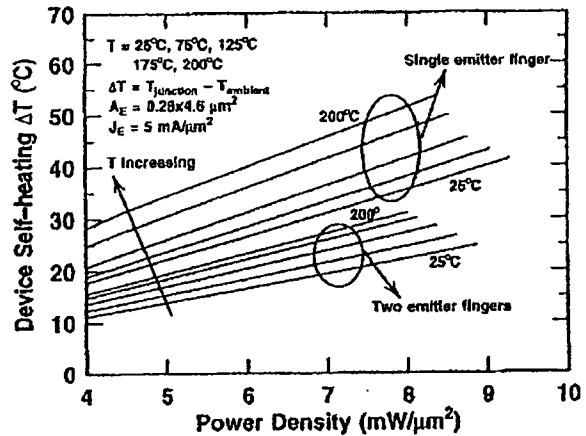

Fig. 24. Device self-heating characteristics at various temperatures for single- and double-stripe devices.

temperature, an increase of M-1 is necessary to offset the β decrease, in agreement with the data. M-1 decreases for the same V_{CB} as temperature increases, due to the increase in phonon scattering with temperature [60]–[62]. Note that for the same biasing current the base-emitter turn-on voltage inherently decreases at higher temperature due to the increase of the intrinsic carrier concentration. Hence, V_{CB} increases with temperature for the same V_{CE}. M-1 is a complicated function of temperature, as is V_{CB} and hence the emitter-base turn-on voltage. Observe that BV_{CEO} of the high-performance devices decreases slightly as the temperature increases, while that for the high-breakdown devices increases with temperature (obviously good news in the latter case). This difference is noteworthy for circuit applications and is the result of the differences in M-1 between the two (the temperature dependence of the β is nearly the same for both). We have also performed compact model simulations (using a calibrated VBIC model) of BV_{CEO} (T), and since that model does not explicitly account for the temperature dependence of M-1, the model does not capture the data particularly well. Thus, existing compact models may need to be refined to accurately capture the high-temperature behavior of these SiGe HBTs.

D. Reliability Issues

Temperature is a well-known, albeit complicated, accelerator for most device failure mechanisms, and thus is a key concern for any high-temperature applications of SiGe HBTs. In addition to simple changes in ambient temperature, transistor self-heating also increases the internal device temperature as well as the temperature gradients, potentially producing additional reliability concerns. Since the increase in phonon scattering with increased temperature will generally degrade the thermal conductivity, this issue is an important consideration for high-temperature electronics. The self-heating characteristics of these SiGe HBTs as a function of ambient temperature were measured using the technique described in [63], and the results are
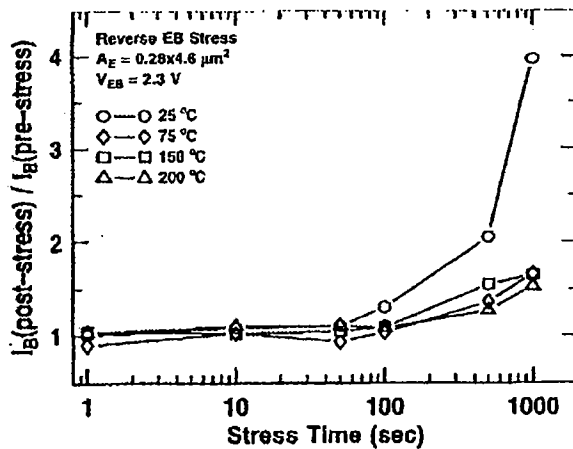
Fig. 25. Base current damage ratio at $V_{BE} = 0.5$ V versus stress time for reverse emitter-base stress at various temperatures.
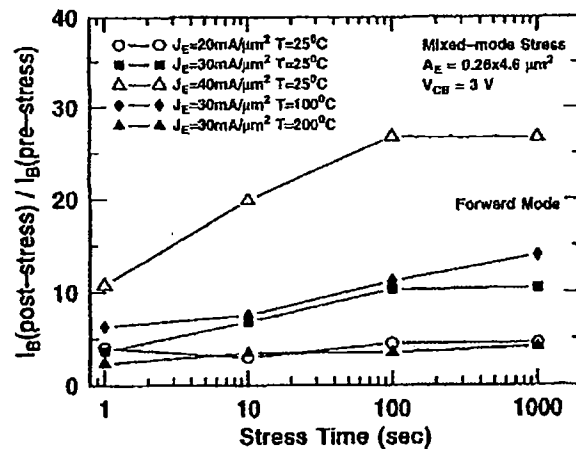

Fig. 26. Base current damage ratio at $V_{BE} = 0.5$ V versus "mixed-mode" stress time for different emitter current densities and different stress temperatures.

shown in Fig. 24. The measured thermal resistance increases as ambient temperature increases, as expected. The model presented in [64] suggests that device self-heating and its thermal resistance can be significantly reduced by breaking the emitter finger into smaller segments and has been confirmed with our data at higher temperatures, as shown in Fig. 24. It should thus be possible to use this approach to help mitigate the impact of high-temperature operation on the device self-heating characteristics.

The effects of reverse emitter-base hot carrier stress is to increase (degrade) the base current without affecting the collector current. Shown in Fig. 25 is the base current damage ratio at different stress temperatures. As the temperature increases from 25 °C to 75 °C, the base current damage ratio decreases, consistent with [65]. As the temperature increases further, however, observe that the base current damage ratio "saturates" for the same stress time. The net temperature dependence of the device degradation depends on the number of injected hot carriers and the energy of those carriers. Under constant stress voltage conditions, the number of hot carriers present at the Si–SiO$_2$ interface is proportional to the reverse-bias stress current, which increases with the ambient temperature. The energies of the carriers, however, depends on the mean free path between the carrier scattering events, which decreases with an increase of the ambient temperature due to enhanced phonon scattering, and thus for these devices, at least between 25 °C and roughly 75 °C, appears to dominate the damage process. Clearly, the reverse EB stress at high temperatures is improved compared to room temperature, which is good news from an application standpoint.

We have previously reported a robust, time-dependent stress methodology for investigating "mixed-mode" (simultaneously forcing of high J_E and high V_{CB}) reliability degradation in SiGe HBTs [66], and this technique has been applied in the current investigation. First, the known J_E dependence at 25 °C was investigated as a reference point for the damage process, and then J_E was fixed at

30 mA/μm^2 and the ambient temperature was increased to 100 °C and 200 °C, respectively. The resultant base current damage ratio for the forward-mode characteristics are shown in Fig. 26. For the forward-mode Gummel characteristics, when J_E is fixed at 30 mA/μm^2 and the ambient temperature increases from 25 °C to 100 °C, the base current damage ratio increases slightly. As the temperature increases further to 200 °C, however, the base current damage ratio actually decreases to the similar damage level as the ratio for mixed-mode stress at room temperature with the J_E of 20 mA/μm^2, which is clearly excellent news. The mixed-mode stress is known to create a large inverse-mode base leakage current component, while reverse EB stress does not create any excess base leakage in the inverse-mode SiGe HBTs [67]. The mixed-mode stress induces traps not only in the EB space-charge region but also in the CB space-charge region, the latter consistent with the observed increase in inverse-mode base current leakage. The base current damage ratio for the inverse-mode Gummel characteristics shows similar changes as that for the forward-mode Gummel characteristics with current density and temperature. This competing damage enhancement and subsequent passivation with increasing stress was also reported in [68]. These results suggest that the effects of the high current stress dominate over those of the ambient temperature alone, consistent with results in [69].

In general, contrary to popular wisdom, we do not see any obvious device-level reliability damage mechanisms in these SiGe HBTs that would be of direct concern for electronics operating at high temperatures. The transistor high-frequency characteristics (i.e., f_T and f_{max}) are essentially unchanged after either stress protocol, to within our measurement accuracy. Although we have not as yet measured it, given that this SiGe technology contains full-copper metallization, electromigration concerns at high temperatures are not expected to be a serious constraint for this technology, but nevertheless needs to be explored in more detail.
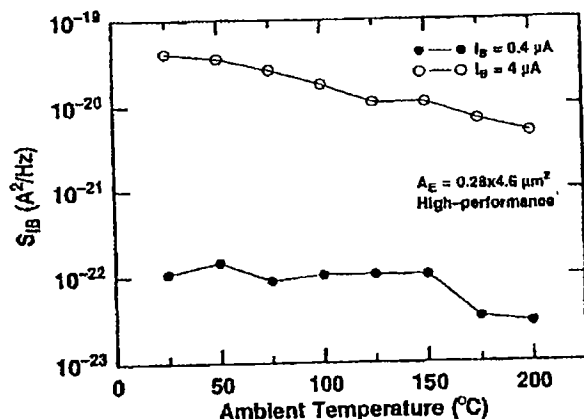
Fig. 27. Low-frequency noise performance at elevated temperatures.

Fig. 28. Forward-mode Gummel characteristics of a 350-GHz SiGe HBT during radiation exposure.

E. Low-Frequency Noise

Low-frequency noise in transistors usually has a $1/f$-like spectrum and sets the lower limit on the signal level, not only in the low frequency range, but also at high frequencies via the up-conversion to the carrier frequency through the nonlinearities of the device. Low-frequency noise is thus a crucial design issue in many analog and RF circuits and systems such as direct-conversion receivers, oscillators, and mixers. Being able to simultaneously achieve very small low-frequency noise and noise figure is one of the unique advantageous features of SiGe HBTs [1]. The input-referred base current noise spectra in SiGe HBTs operating at high temperatures with I_B of 0.4 and 4 μA was measured, and Fig. 27 shows S_{I_B} at 10 Hz as the temperature increases. As can be seen clearly from the results, LFN actually improves with increased temperature—again, clearly good news.

VII. RADIATION EFFECTS

The "holy grail" in the realm of space electronics can be viewed as a conventional terrestrial IC technology with a SoC capability, which is also radiation-hard as fabricated, without requiring any additional (costly) process modifications or layout changes. It is within this context that we discuss SiGe HBT BiCMOS technology as potentially such a "radiation-hard-as-fabricated" IC technology with possibly far-ranging implications for the space community.

A. DC Effects

The response of SiGe HBTs to a variety of radiation types has been reported, including gamma rays, neutrons, and protons [71]–[77]. Since protons induce both ionization and displacement damage, they can be considered the worst case for radiation tolerance. For the following results, a relevant proton energy of 63 MeV was used. At proton fluences of $\times 10^{12}$ p/cm^2 and 5×10^{13} p/cm^2, the measured equivalent total ionizing dose (TID) was approximately 135 and 6759 krad(Si), respectively, the latter being far larger than
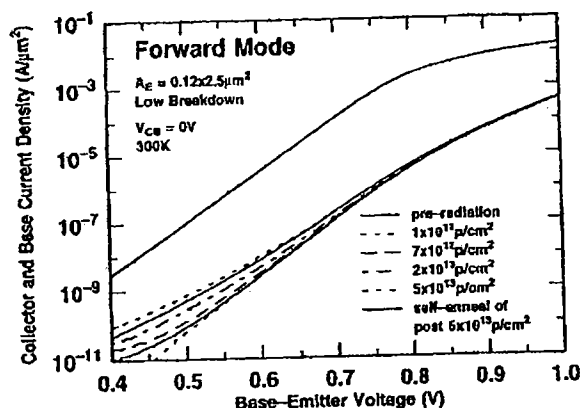
most orbital missions require, and hence is a worst case exposure level.

The typical response of a SiGe HBT to irradiation can be seen in Fig. 28, which shows typical measured Gummel characteristics of a fourth-generation SiGe HBT, both before and after exposure to protons [71]–[77]. As expected, the base current increases after a sufficiently high proton fluence due to the production of G/R trapping centers, and hence the current gain of the device degrades. There are two main physical origins of this degradation. The base current density is inversely proportional to the minority carrier lifetime in the emitter, so that a degradation of the hole lifetime will induce an increase in the base current. In addition, ionization damage due to the charged nature of the proton fluence produces interface states and oxide trapped charges in the spacer layer at the emitter-base junction. These G/R centers also degrade I_B, particularly if they are placed inside the EB space-charge region, where they will yield an additional non-ideal base current component (non-kT/q exponential voltage dependence). By analyzing a variety of device geometries, it can be shown that the radiation-induced excess base current is primarily associated with the EB spacer oxide at the periphery of the transistor, as naively expected, and is hence the radiation response is dominated by ionization damage rather than displacement damage. The radiation-induced degradation of the base current and current gain for four generations of SiGe technology are shown in Figs. 29 and 30. Less than 30% degradation in peak current gain is observed across all four technology nodes, to 1.0 Mrad(Si) equivalent radiation levels, suggesting that SiGe HBTs are robust to TID for typical orbital proton fluences for realistic circuit operating currents above roughly 100 μA without any additional radiation hardening. These results are significantly better than for conventional diffused or even ion-implanted Si BJT technologies (even radiation-hardened ones).

Of particular interest is the inference of the spatial location of the proton-induced traps in these devices [73]. The existence of proton-induced traps in the EB space-charge region is clearly demonstrated by the G/R-induced increase in
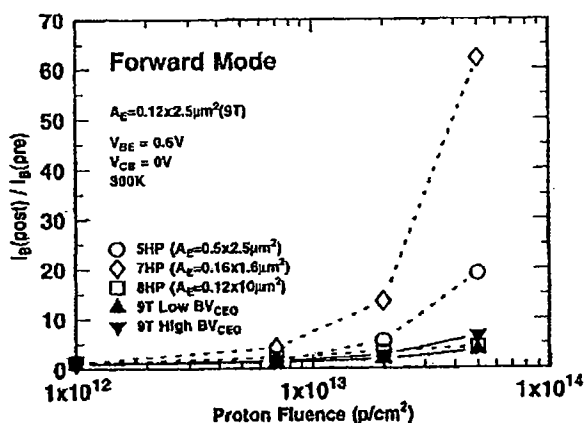
Fig. 29. Normalized forward base current degradation for first-generation (5HP), second-generation (7HP), third-generation (8T), and fourth-generation (9T) SiGe technology nodes.

Fig. 31. Pre- and postradiation cutoff frequency versus bias current density for first-generation (5HP), second-generation (7HP), third-generation (8T), and fourth-generation (9T) SiGe technology nodes.
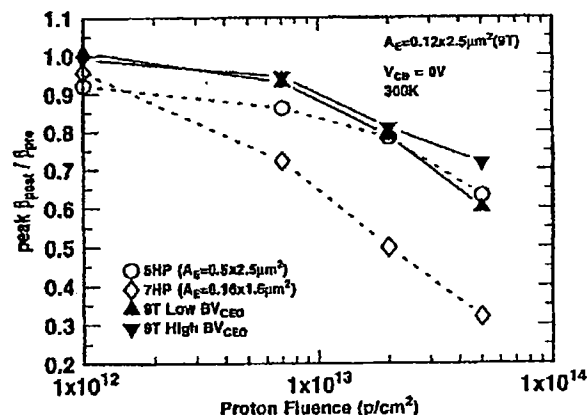

Fig. 30. Current gain degradation for first-generation (5HP), second-generation (7HP), third-generation (8T), and fourth-generation (9T) SiGe technology nodes.

Fig. 32. Extracted minimum noise figure of a first-generation SiGe HBT as a function of proton fluence for multiple frequencies.

B. AC Small-Signal and Noise Effects

To assess the impact of radiation on the ac performance of the transistors, the S-parameters were measured to 40 GHz both before and after proton exposure [78]. From the measured S-parameters, the transistor cutoff frequency as a function of bias current density can be extracted, and is shown for four technology generations in Fig. 31. Only a slight degradation in f_T (and f_{max}) is observed, the latter being expected from the minor increase of the base resistance with irradiation, due to either carrier removal, mobility/lifetime changes, or both. The broad-band noise performance of SiGe HBTs is critical for space-borne transceivers and communications platforms. As shown in Fig. 32 the minimum noise figure (NF_{min}) degrades only slightly at 2.0 GHz in a first-generation SiGe HBT after an extreme proton fluence of 5×10^{13} p/cm^2 (from 0.95 dB to a still-excellent value of 1.07 dB, a 12.6% degradation).

SiGe HBTs have the desirable feature of low $1/f$ noise commonly associated with Si bipolar transistors, which is of great importance because upconverted low-frequency noise (phase noise) typically limits the spectral purity of communication systems. Understanding the effects of radiation on $1/f$ noise in SiGe HBTs thus becomes a crucial issue

the nonideal base current component shown in the Gummel characteristics. The existence of radiation-induced traps in the collector-base space-charge region was verified by measuring the inverse mode Gummel characteristics of the device (emitter and collector leads swapped). In this case the radiation-induced traps in the CB junction now act as G/R centers in the inverse EB junction, with a signature non-kT/q exponential slope. Two-dimensional (2-D) simulations were calibrated to both measured data for the pre- and postirradiated devices at a collector-base voltage of 0.0 V. In order to obtain quantitative agreement between the simulated and measured irradiated results, traps must be located uniformly throughout the device, and additional interface traps must be located around the emitter-base spacer oxide edge. Most of the radiation-induced recombination occurs inside the EB space-charge region, leading to a nonideal base current, as expected.
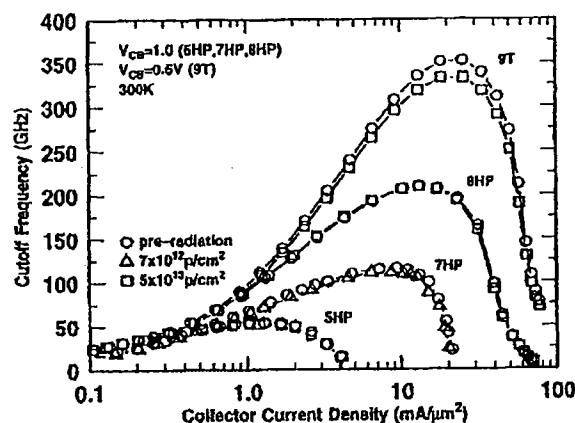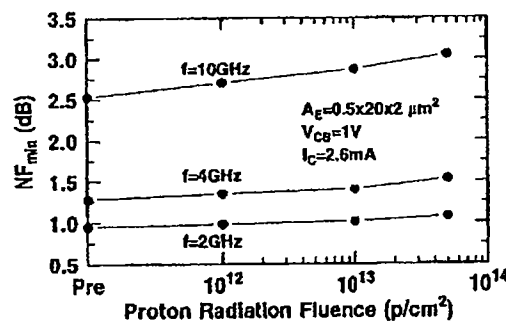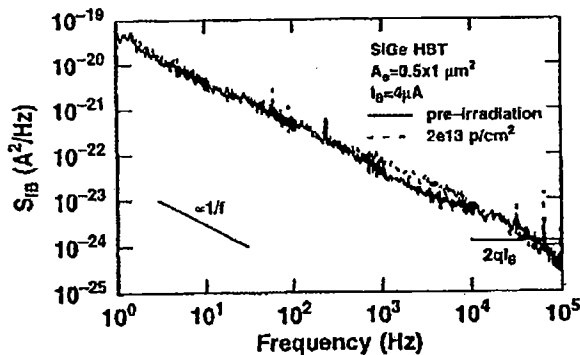
Fig. 33. Input-referred base current PSD for a first-generation 0.5 × 1.0 μm^2 transistor, before and after irradiation.

Fig. 34. Normalized base current as a function of gamma radiation dose rate, for both Si BJTs and first-generation SiGe HBTs.

for space-borne communications electronics. Physically, $1/f$ noise results from the presence of G/R center traps in the transistors, from which trapping–detrapping processes occur while carriers flow inside the device, thus modulating the number of carriers (and hence currents) to produce $1/f$ noise. The preirradiation low-frequency noise spectrum in these SiGe HBTs is typically $1/f$, with an I_B^2 dependence, while $S_{I_B} \times A_E$ is almost independent of A_E. The I_B^2 and $1/A_E$ dependencies of S_{I_B} are strong indicators of uniformly distributed noise sources over the entire emitter area. After 2×10^{13} p/cm^2 proton irradiation, the low-frequency noise spectrum in first-generation SiGe HBTs remains $1/f$ in frequency dependence, and free of G/R (burst) noise, and at roughly the same noise magnitude (i.e., no radiation-induced degradation), as can be seen in Fig. 33 [79].

C. Origin of Radiation Hardness

We note that careful comparisons between identically fabricated SiGe HBTs and Si BJTs (same device geometry and wafer lot, but without Ge in the base for the epitaxial-base Si BJT), show that the extreme level of total dose tolerance of SiGe HBTs is not *per se* due to the presence of Ge [73]. That is, the proton response of both the epitaxial base SiGe HBT and Si BJT are nearly identical. We thus attribute the observed radiation hardness to the unique and inherent structural features of the device itself, which from a radiation standpoint can be divided into three major aspects: 1) in these epitaxial base structures, the extrinsic base region is very heavily doped ($> 5 \times 10^{19}$ cm^{-3}) and located immediately below the emitter-base (EB) spacer oxide region, effectively confining any radiation-induced damage, and its effects on the EB junction; 2) the EB spacer, known to be the most vulnerable damage point in conventional BJT technologies, is thin (< 0.20 μm wide) and composed of an oxide/nitride composite, the latter of which is known to produce an increased level of radiation immunity; and 3) the active volume of these transistors is very small (emitter stripe width $W_E = 0.5$ μm, and base width $W_b < 150$ nm), and the emitter, base, and collector doping profiles are quite heavily doped, effectively lessening the impact of displacement damage. We also note that these SiGe HBTs compare very favorably in both performance and radiation hardness with (more expensive)
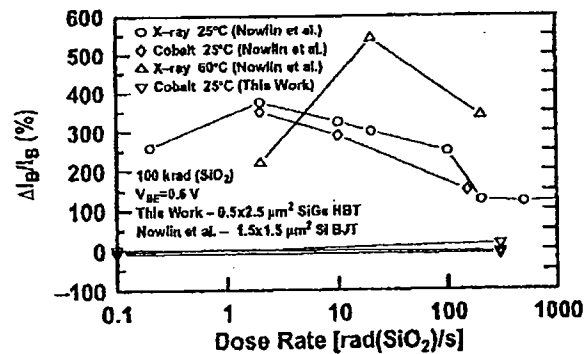
GaAs HBT technologies that are often employed in space applications requiring both very high speed and an extreme level of radiation immunity [80].

D. Low-Dose-Rate Effects

Within the past few years, a pronounced low-dose-rate sensitivity to gamma irradiation that is not screened by the current test methods for ionizing radiation has been observed in Si bipolar technologies. The enhancement in device and circuit degradation at low gamma dose rates has come to be known as enhanced low-dose-rate sensitivity (ELDRS) [81]–[83]. The ELDRS effect was first reported in 1991, which demonstrated that existing radiation hardness test assurance methodologies were not appropriately considering worst case conditions. The physical origins underlying ELDRS have been hotly debated for years, and numerous mechanisms proposed. Recent attempts to understand ELDRS include a model suggesting that the lower net radiation induced trapped charge density at high dose rates is a result of a space-charge phenomenon, caused by delocalized hole traps which occur in heavily damaged oxides such as bipolar base oxides. These traps can retain holes on a timescale of seconds to minutes, causing a buildup of positive charge in the oxide bulk during high-dose-rate irradiation. This is in contrast to low-dose-rate irradiation, where the irradiation time is much longer, effectively allowing the holes in the trap centers to be detrapped. Thus, in the high-dose-rate case, the larger total trapped hole density forces holes near the interface to be trapped closer to the interface, where they can be compensated by electrons from the silicon. This lowers the resultant net trapped charge density.

To assess ELDRS in first-generation SiGe technology, low-dose-rate (0.1 rad(Si)/s) and high-dose-rate (300 rad(Si)/s) experiments were conducted using cobalt-60 [84]. As can be seen in Fig. 34, low-dose-rate effects in these first-generation SiGe HBTs were found to be nearly nonexistent, in striking contrast to reports of strong ELDRS in conventional Si bipolar technologies. We attribute this observed hardness to ELDRS to the same mechanisms responsible for the overall radiation hardness of the technology and is likely more structural in nature than due to

Table 2
Impact of Radiation Exposure Uisng 63-MeV Protons on Various
SiGe Analog, RF, and Passive Circuits

SiGe HBT Circuit	Parameters	Pre-radiation	After 5x10^{15} p/cm^2	Units
Bandgap Reference	V_{cc}	3.0	3.0	V
	I_{cc}	0.773	0.767	mA
	V_{bm} at 300K	1.37416	1.372096	V
	Stability (-55 to 85°C)	81.2	81.7	ppm/°C
Voltage Controlled Oscillator	Frequency	5.0	5.0	GHz
	V_{cc}	3.3	3.3	V
	I_{cc}	22.5	22.5	mA
	Output Power	-5.0	-5.5	dBm
	Phase Noise	-112.5	-111.9	dBc/Hz
	Tuning Range	4,595-5,452	4,623-5,470	MHz
LC Bandpass Filter	Frequency	1.9	1.9	GHz
	Filter Q (@ 3dB BW)	7.6	7.6	-
	Insertion Loss	16.8	16.8	dB
	L	2.5	2.5	nH
	Inductor Q	7.4	7.4	-
	C	6.0	6.0	pF
	Capacitor Q	58	58	-

any unique advantage afforded by the SiGe base. Interestingly, an anomalous decrease in base current was also found in these devices at low dose rates, suggesting that a new physical phenomenon is present at low dose rates in these devices.

E. SiGe HBT Circuit Tolerance

For the successful deployment of SiGe technology into space-based systems, circuit-level radiation hardness is clearly more important than device-level hardness. As presented above, the TID device degradation is minor in the bias range of interest to most actual circuits (typically $I_C > 100\ \mu A$). In order to assess the impact of radiation exposure on actual first-generation SiGe HBT circuits, we have compared two very important, yet very different circuit types, one heavily used in analog ICs (the bandgap reference circuit), and one heavily used in RFICs (the voltage controlled oscillator) [85], [86]. Each circuit represents a key building block for realistic SiGe ICs that might be flown in space. Each of these SiGe HBT circuits was designed using fully calibrated SPICE models, laid out, and then fabricated on the same wafer to facilitate unambiguous comparisons. In addition, because any realistic RFIC must also necessarily include passive elements such as monolithic inductors and capacitors, we have also investigated the effects of proton exposure on an RF LC bandpass filter. As can be seen from the data (Table 2), the impact of even extreme proton lluences has minimal effect on either the output voltage or temperature sensitivity of BGRs, the phase noise or tuning range of VCOs or passive elements, and is indicative of the overall robustness of this SiGe technology for analog and RF circuit applications. More recent work on radiation damage in 60-GHz millimeter-wave transceiver building blocks exhibits a comparable total dose robustness [87].

F. Single Event Upset (SEU)

Clearly, a space-qualified IC technology must demonstrate sufficient SEU immunity to support high-speed circuit applications as well as possess total dose tolerance. It is well known that even III-V technologies that have significant TID tolerance often suffer from poor SEU immunity, particularly at high data rates. Recently, high-speed SiGe HBT digital logic circuits were found to be vulnerable to SEU at even low linear energy transfer (LET) values [88]-[90]. In addition, successfully employed III-V HBT circuit-level hardening schemes using the current-sharing hardening (CSH) technique were found to be ineffective for these SiGe HBT logic circuits (Fig. 35). To understand single event effects in SiGe HBTs, one must use calibrated 2-D/three-dimensional (3-D) device simulation to assess the charge collection characteristics of SiGe HBTs. These device-level simulation results can then be coupled to circuit-level modeling to better understand circuit-level mitigation approaches. From a device perspective, it is important to first assess the transistor charge collection characteristics as a function of terminal bias, load condition, substrate doping, and ion strike depth [91], [92]. Bias and loading conditions were chosen to mimic representative circuit conditions within an actual ECL/CML digital circuit. Fig. 36 shows the charge collected by the collector versus time for different RC loads. The base and emitter terminals were grounded, the substrate bias was -5.2 V, the collector was connected to ground through an RC load, and the substrate doping was 5×10^{16} cm^{-3}. A uniform LET of 0.1 pC/μm (equivalent to 10 MeV-cm^2/mg) over 10 m depth was used, which generates a total charge of 1.0 pC. The results clearly show that charge collection is highly dependent on the transistor load condition (i.e., circuit topology). As the load resistance increases, the collector-collected charge decreases. Note, however, that the emitter-collected charge increases correspondingly. The underlying physics is that more electrons exit through the emitter, instead of the collector. A larger load resistance presents a higher impedance to the electrons at the collector, and thus more electrons exit through the emitter. The collector of the adjacent device only collects a negligible amount of charge, despite the transient current spikes of the strike. Nearly all of the electrons deposited are collected by the collector and the emitter, although the partition between emitter and collector collection varies with the load condition. The impact on the SiGe base layer on the charge collection properties is a secondary effect.

To better understand circuit-level SEU response, we combined these simulated current-time profiles with circuit-level modeling on different SiGe HBT latch architectures [93]. Clear differences in SEU response can be observed between various latches (a brute-force NAND implementation being best, and the popular master-slave configuration being worst). This modeling methodology suggests that circuit-level mitigation techniques should be useful in SEU hardening of SiGe HBT logic, albeit at some level of additional power dissipation and circuit complexity. A potential SEU-hardening approach has been recently discussed in [94], but clearly more research is needed in the area of SEU mitigation before widespread deployment of SiGe circuitry in space is attempted, and that work is (aggressively) ongoing.
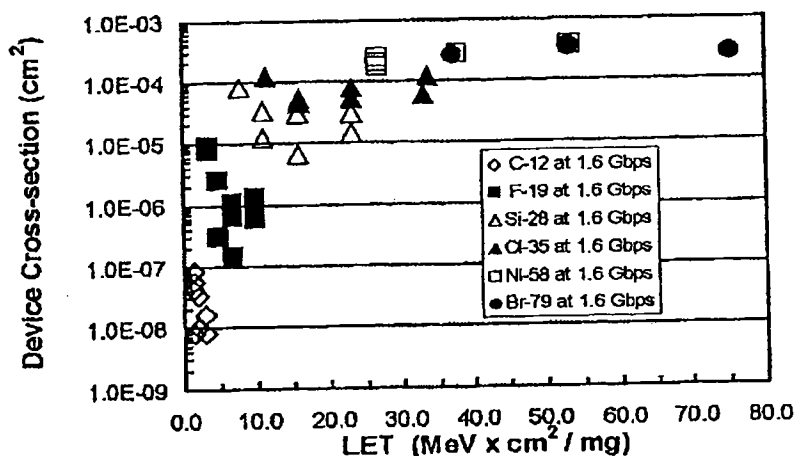
Fig. 35. Experimental SEU cross section test data on first-generation SiGe HBT shift registers (after [88]).
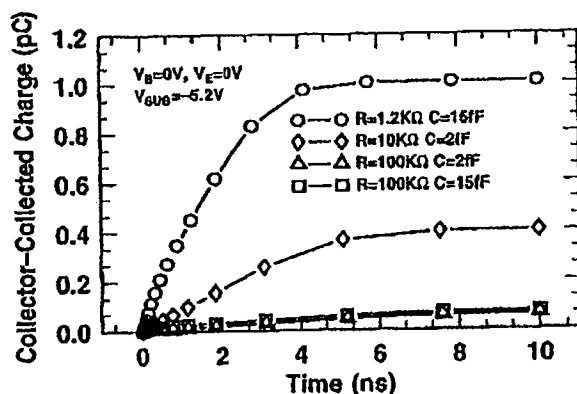

Fig. 36. Simulated collector-collected charge versus time for different RC loads for first-generation SiGe HBT.

VIII. CONCLUSION

"Extreme environments" represents an important niche market for electronics and spans the operation of electronic components in surroundings lying outside the domain of conventional commercial, or even military, specifications. Such extreme environments would include, for instance, operation to very low temperatures (e.g., to 77 K or even 4.2 K), operation at very high temperatures (e.g., to 200 °C or even 300 °C), and operation in a radiation-rich environment (e.g., space). We have argued that the unique bandgap-engineered features of SiGe HBTs offer great potential to simultaneously satisfy all three extreme environment applications, potentially with little or no process modification, ultimately providing compelling cost advantages at the IC and system level.

The relevant industrial and government drivers in the extreme environment electronics community are beginning to perk up their ears to the possibilities of SiGe technology, especially so for space electronics. These customers are in turn approaching the SiGe foundries for these types of needs, and beginning to actually design and build SiGe ICs with an end goal of system insertion in mind. Defense and government funding agents are supporting the effort. These are all clearly good signs. This is not to say, however, that the battle is won. Much remains to be done in the research arena. As argued here, many "proof-of-concept" measurements have been conducted demonstrating the efficacy of SiGe HBTs for the radiation environment, cryogenic electronics, and high temperature. As anyone in industry knows, however, going from proof-of-concept to system-level products is a very different thing. "Open issues" in the field of SiGe for extreme environment electronics that require attention include the following.

- While many device-level demonstrations have been published, more circuit-level demonstrations need to be conducted to explore the complex interaction space between devices in circuits in extreme environments.
- New circuit design techniques are needed for developing mixed-signal electronics that will function not just at 77 K or at 200 °C, but from 77 K to 200 °C. These are very different circuit design problems. When one throws in the added variable of desiring operation from 77 K to 200 °C, but now in a radiation environment, you have an even more serious design challenge. These aspects have only begun to be addressed, and will require dedicated effort.
- Reliability at cryogenic temperatures must be explored in more detail. Particularly in scaled SiGe HBTs, new impact ionization triggered device degradation mechanisms have been observed and should give pause for thought in low-temperature conditions where carrier mean free path lengths are considerably longer.
- Reliability at high temperatures must be explored in more detail. While 200 °C may be currently manageable, changes to interconnect and metallization chemistry at 300 °C is a valid concern.

- SEU is perhaps the most looming Achilles' heel for SiGe in space applications. While this is largely a concern for digital logic at present, transient phenomena in analog and RF blocks is clearly also something to be worried about. Dedicated research aimed at mitigation SEU approaches is heavily underway and must be relentlessly pursued until acceptable solutions are found. We should note that SiGe HBT technology fabricated on SOI substrates should in principle offer significant leverage in the context of SEU mitigation for SiGe (and also offer potential advantages for high-temperature operation as well). There have, in fact, been recent (encouraging) radiation results presented on SiGe HBTs fabricated on both thick-film and (SOI CMOS-compatible) thin-film SOI substrates [95], [96]. This SiGe-on-SOI SEU mitigation path clearly has some cost disadvantages associated with it, but is worthy of attention, especially if SEU mitigation paths in bulk SiGe technologies prove overly challenging.

- Given that the CMOS side of SiGe HBT BiCMOS technology is a compelling advantage for highly integrated (SoC) systems, more work is needed on the CMOS components for extreme environments, particularly as a function of technology scaling. What may look good at first generation may not look so good at third generation.

- Design tools for robust circuit design for extreme environments is painfully lacking at present. Even foundry-available device compact models are typically only valid over the mil-spec temperature range (at best) and do not include radiation effects. System-level design and optimization tools are virtually nonexistent.

- Finally, we have made little mention here of the packaging and testing needs to support extreme environment electronics. There are no systems without robust packages or means to test the packaged parts, and this will require significant effort given the often large thermal mismatch between commonly used packaging materials.

Are these "open issues" potential show-stoppers? Probably not. Do they need to be solidly addressed by the community as deployment of SiGe technology for extreme environment applications accelerates. Absolutely. Let the games begin!

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